C. Appendix 3 – Combinational Shifter Implementation

A shifter can also be implemented as a sequence of multiplexers. In such an implementation, the output of one MUX is connected to the input of the next MUX in a way that depends on the shift distance. The number of multiplexers required for an n-bit word is $n * \log_2 n$.

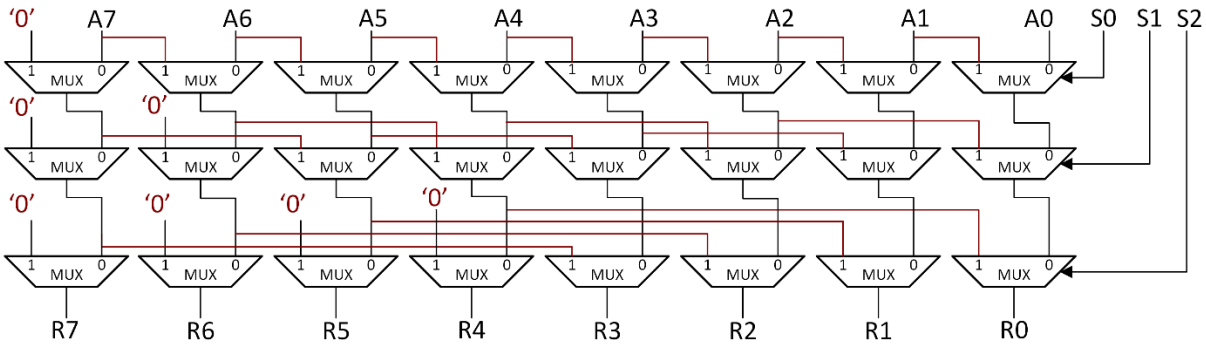

Figure C-1: Multi-level (logarithmic) 8-bit right shifter

Example:

- sw(4 downto 0) is a 5-bit signal that can be shifted left or right arithmetic
- sw(6:5) is the shift amount: 0, 1, 2 or 3 positions
- sw(7) is the shift direction
  - sw(7) = 0 – shift left
  - sw(7) = 1 – shift right arithmetic
- the result is displayed on the LEDs from the development board

The code in VHDL implemented with two processes:

```
process(sw)
begin
   if sw(5) = '1' then    -- shift with 1 position
      if sw(7) = '0' then
         shift1 <= sw(3 downto 0) & '0';           -- shift left
      else
         shift1 <= sw(4) & sw(4 downto 1);       -- shift right arithmetic
      end if;
   else
      shift1 <= sw(4 downto 0);
   end if;
end process;

process(sw, shift1)
begin
   if sw(6) = '1' then    -- shift with 2 position
      if sw(7) = '0' then
         shift2 <= shift1(2 downto 0) & "00";                    -- shift left
      else
         shift2 <= shift1(4) & shift1(4) & shift1(4 downto 2);   -- shift right arithmetic
      end if;
   else
      shift2 <= shift1;
   end if;
end process;

led <= shift2;
```