



Computer Architecture

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2nd Year, Computer Science

Lecture 12: Modern CPU Architectures

<http://users.utcluj.ro/~negrum/>



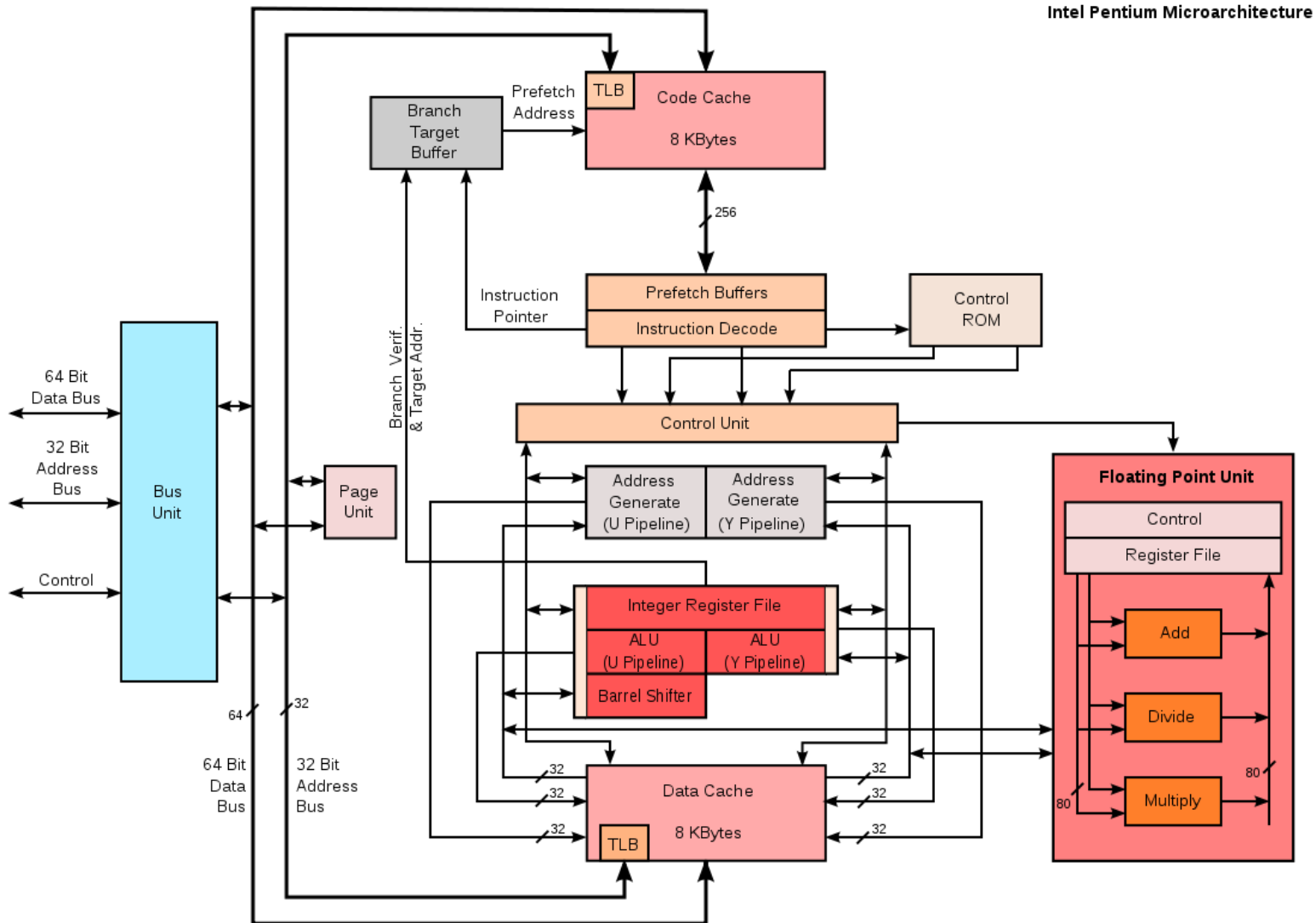
Intel Processor History – Single Cores



Intel Processor	Year	Data	Technology	Instruction Set	CPU Clock
8008	1972	8-bit	10 μm	8008	0.2 – 0.8 MHz
8080	1974	8-bit	6 μm	8080	2 MHz
8086	1976	16-bit	3.2 μm	x86-16	5 – 10 MHz
80186	1982	16-bit	3.2 μm	x86-16	6 – 25 MHz
80286	1982	16-bit	1.5 μm	x86-16	6 – 25 MHz
80386	1985	32-bit	1 – 1.5 μm	x86 (IA-32)	12 – 40 MHz
80486	1989	32-bit	0.6 – 1 μm	x86 (x87 – FP)	16 – 150 MHz
Pentium (P5)	1993	32-bit	0.8 μm	IA-32	60 – 100 MHz
Pentium Pro (P6)	1995	32-bit	0.35 μm	IA-32	150 – 200 MHz
Pentium MMX	1996	32-bit	0.18 – 0.35 μm	IA-32, MMX	120 – 233 MHz
Pentium II (P6)	1997	32-bit	0.35 μm	IA-32, MMX	233 – 450 MHz
Pentium III (P6)	1999	32-bit	0.13 – 0.25 μm	IA-32, MMX, SSE	450 MHz – 1.4 GHz
Pentium IV (Netburst)	2000	32-bit	0.18 μm	IA-32, MMX, SSE, SSE2, ...	1.3 – 3.8 GHz

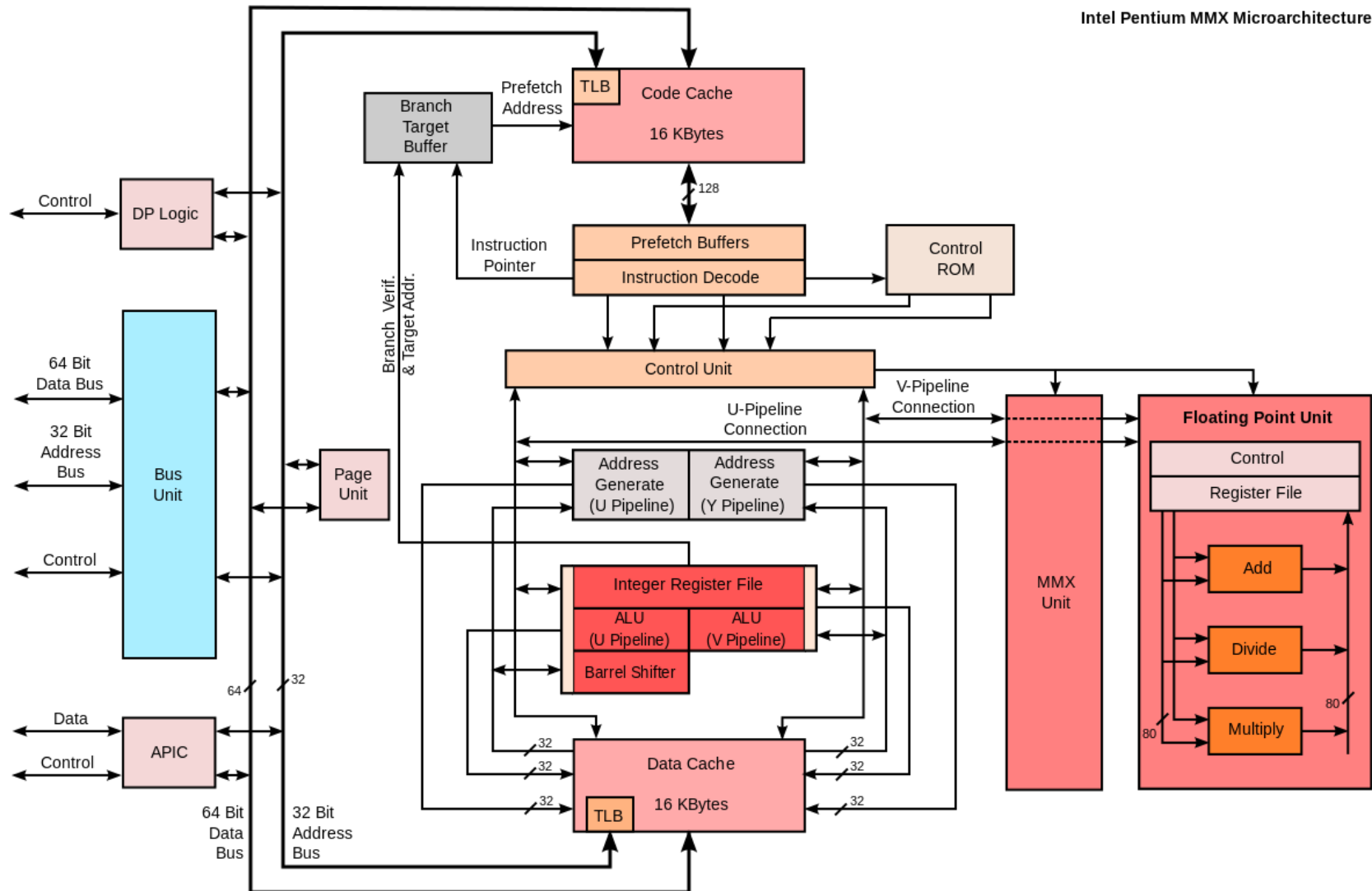


Intel Pentium MicroArchitecture





Intel Pentium MMX MicroArchitecture





NetBurst MicroArchitecture



Pentium IV	Year	Data	Technology	Instruction Set	CPU Clock	Cores
Willamette	2000	32-bit	180 nm	IA-32, MMX, SSE, SSE2	1.3 – 2 GHz	1
Northwood	2002	32-bit	130 nm	IA-32, MMX, SSE, SSE2	1.6 – 3.06 GHz	1
Prescott	2004	64-bit	130 nm	MMX, ..., SSE3, x86-64	2.66 – 3.8 GHz	1
Hyper-Threading Technology – Virtual Cores						
Northwood	2003	32-bit	130 nm	IA-32, MMX, SSE, SSE2	3.06 GHz	1
Prescott	2005	64-bit	90 nm	MMX, ..., SSE3, x86-64	2.66 – 3.8 GHz	1
Cedar Mill	2006	64-bit	65 nm	MMX, ..., SSE3, x86-64	3 – 3.6 GHz	1

Major Issues:

- Large number of pipeline stages: 20 – 31
- power consumption
- heat dissipation



The End of the Single Core Era

Pentium D	Year	Data	Technology	Instruction Set	CPU Clock	Cores
Smithfield	2005	64-bit	90 nm	MMX, ..., SSE3, x86-64	2.66 – 3.73 GHz	2
Pressler	2006	64-bit	65 nm	MMX, ..., SSE3, x86-64	2.66 – 3.73 GHz	2



Intel Tick-Tock Era



- Tick – Shrink
 - Shrinking in the process technology of the previous Intel MicroArchitecture
 - Can introduce new instructions
 - Can make the processor more efficient, more powerful
- Tock – Innovate
 - a new MicroArchitecture
- Every 12 – 18 months → a new tick / tock
- MicroArchitectures:
 - Netburst, P6
 - Core
 - Nehalem
 - Sandy bridge
 - Haswell
 - Skylake



Intel Tick-Tock Era



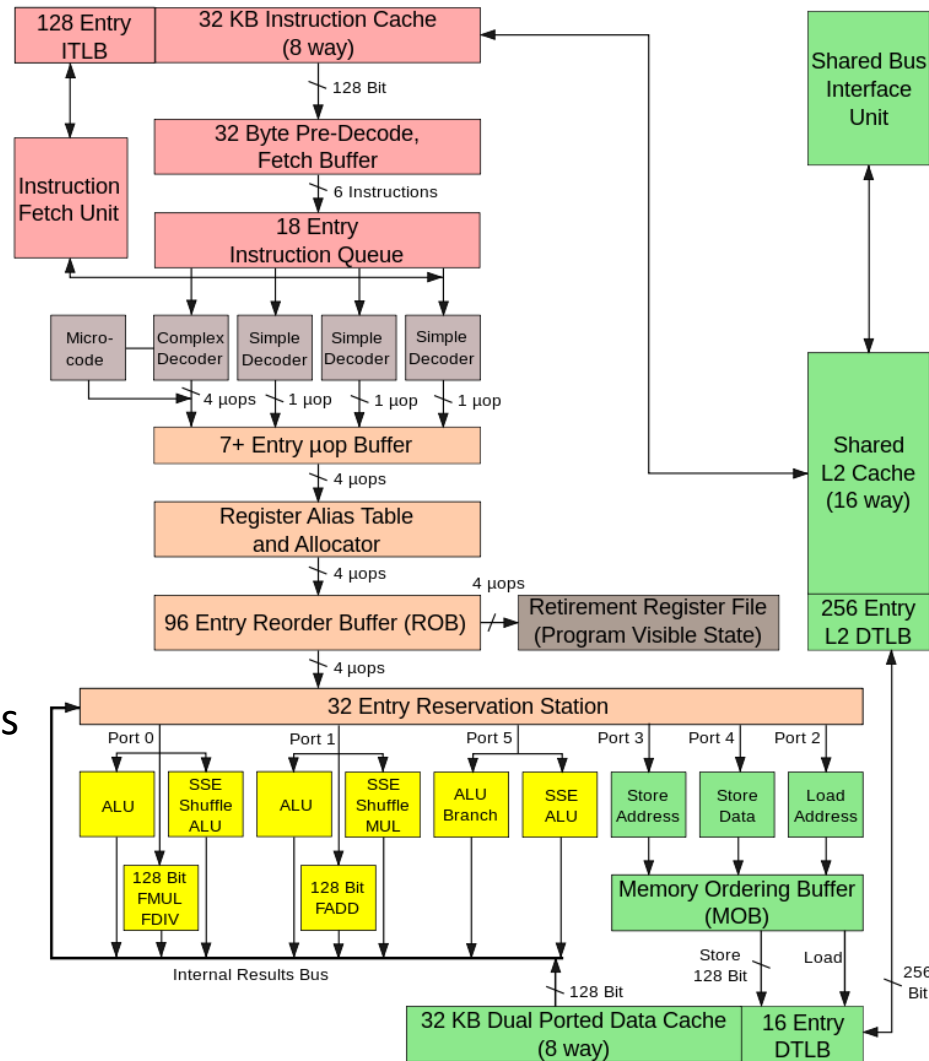
Change	Technology	MicroArchitecture	Code Names	Year	Processors
Tick	65 nm	P6, Netburst	Pressler, Cedar Mill	2006	Core, Pentium 4, Pentium D, Pentium M, Pentium Dual-Core
Tock	65 nm	Core	Merom	2006	Core 2, Pentium Dual- Core
Tick	45 nm		Penrym	2007	
Tock	45 nm	Nehalem	Nehalem	2008	Core i3, i5, i7, ...
Tick	32 nm		Westmere	2010	
Tock	32 nm	Sandy Bridge	Sandy Bridge	2011	Core i3, i5, i7 – 2 nd , ...
Tick	22 nm		Ivy Bridge	2012	Core i3, i5, i7 – 3 rd , ...
Tock	22 nm	Haswell	Haswell	2013	Core i3, i5, i7 – 4 th , ...
Tick	14 nm		Broadwell	2014	Core i3, i5, i7 – 5 th , ...
Tock	14 nm	Skylake	Skylake	2015	Core i3, i5, i7 – 6 th , ...
Tock	14 nm		Kaby lake	2017	Core i3, i5, i7 – 7 th , ...
Tock	14 nm		Coffee Lake	2018	Core i3, i5, i7 – 8 th , ...
Tick	10 nm		Cannonlake	2019	??
Tock	10 nm	Ice Lake	Ice Lake	2019	??



Intel Core 2 MicroArchitecture



- Number of Cores
 - 1, 2, 4
 - No Hyper-threading
 - 14-stage pipeline
 - 4 decoders – 7 μ Ops
 - Cache memory
 - L1: 32 KB data
 - L1: 32 KB instr.
 - L2: 256 KB
 - Scheduler – 32 entries
- 6 μ Operations / cycle



retirement bandwidth
4 μ Operations / cycle

Intel Core 2 Architecture



Nehalem MicroArchitecture

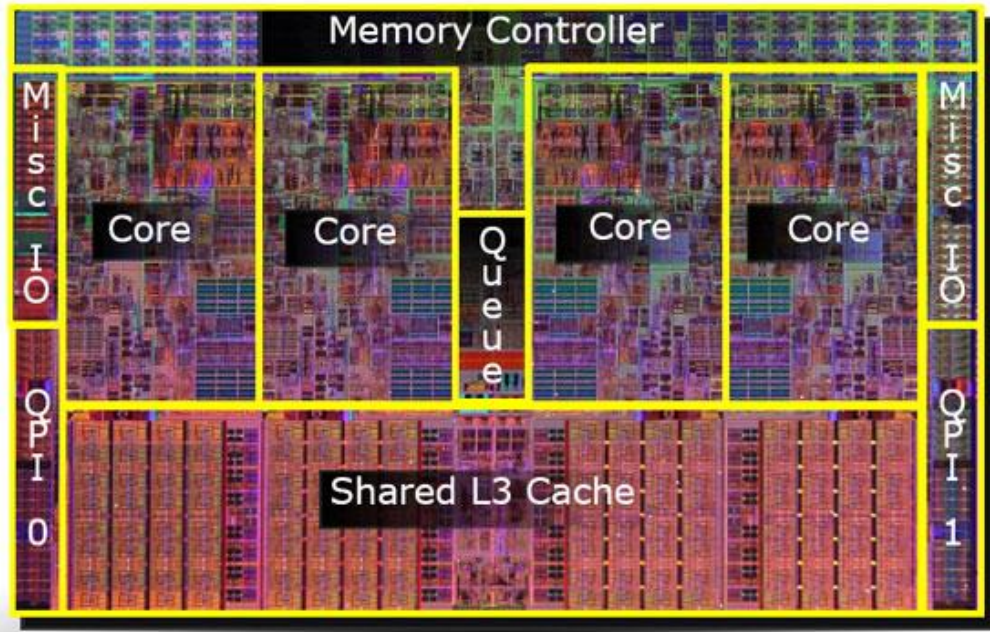


- Increased parallelism over Core MicroArchitecture
- Increased resources for higher performance
- Intel turbo Boost Technology – increases frequency when possible
 - Higher performance on demand
- **Intel Hyper-Threading Technology** – more threads than cores
- New Instructions – SSE 4.2

Structure	Merom (Core)	Nehalem
Reservation Station	32	36
Load buffers	32	48
Store buffers	20	32
Cache Layers	2	3
L1 cache	32 KB instruction 32 KB data	32 KB instruction 32 KB data
L2 cache	256 KB instr+data	256 KB instr+data
L3 cache – shared	None	Up to 8 MB



Nehalem MicroArchitecture

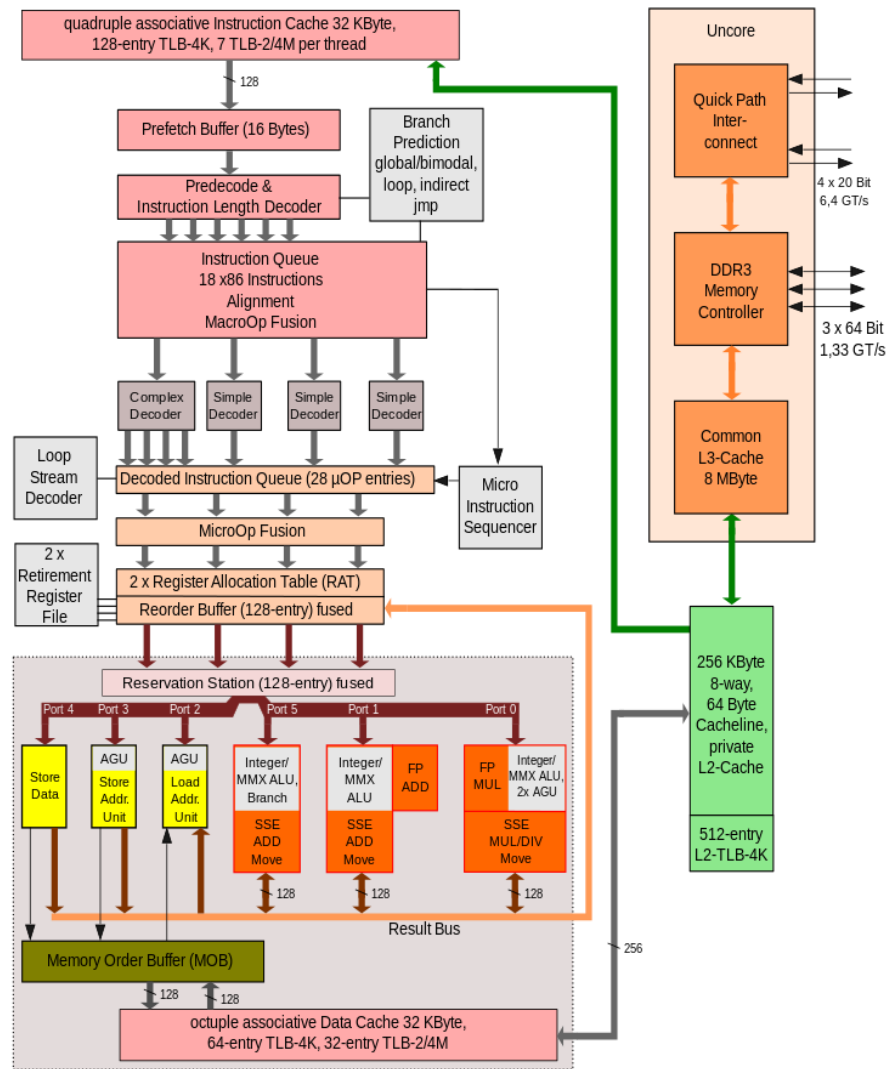


Nehalem MicroArchitecture

Part of the NorthBridge → CPU
QPI – Quick Path Interconnect

Nehalem's Core Architecture

Intel Nehalem microarchitecture



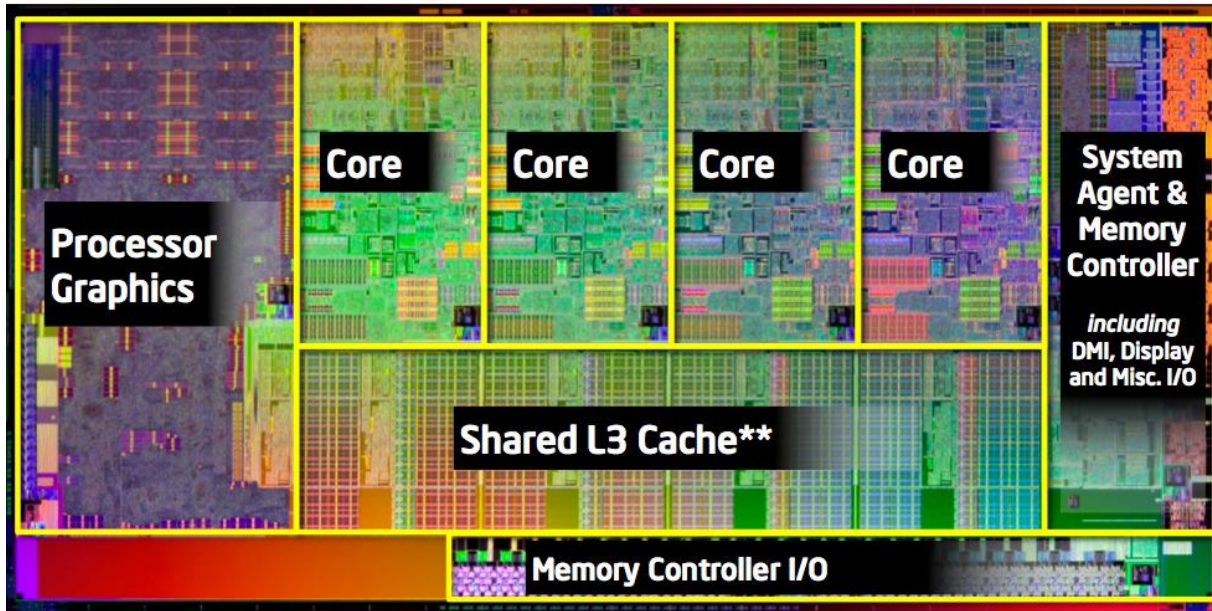
GT/s: gigatransfers per second



Intel Sandy Bridge



Sandy Bridge
Tock – 32 nm

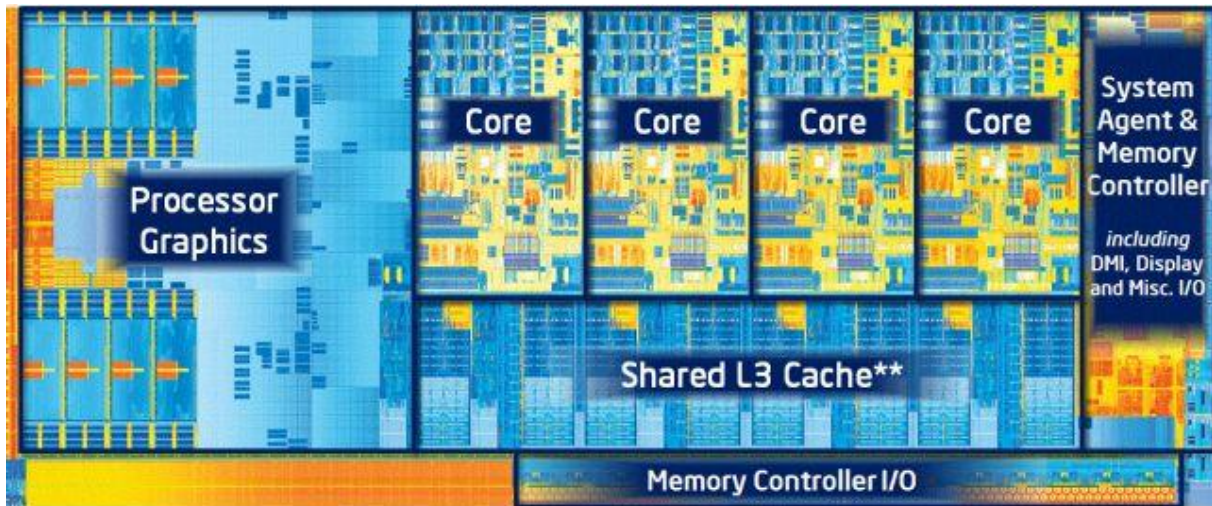


Memory Controller and Graphics

inside CPU



Ivy Bridge
Tick – 22 nm



System on Chip
SoC



Intel Sandy Bridge



- Increased graphics performance
- Enhanced security capability
- New instructions – Advanced Vector Extension (AVX)
- Intel Dynamic Execution for Core
 - In-order issue
 - Speculative, super-scalar, out-of-order execution
 - 14 stage pipeline

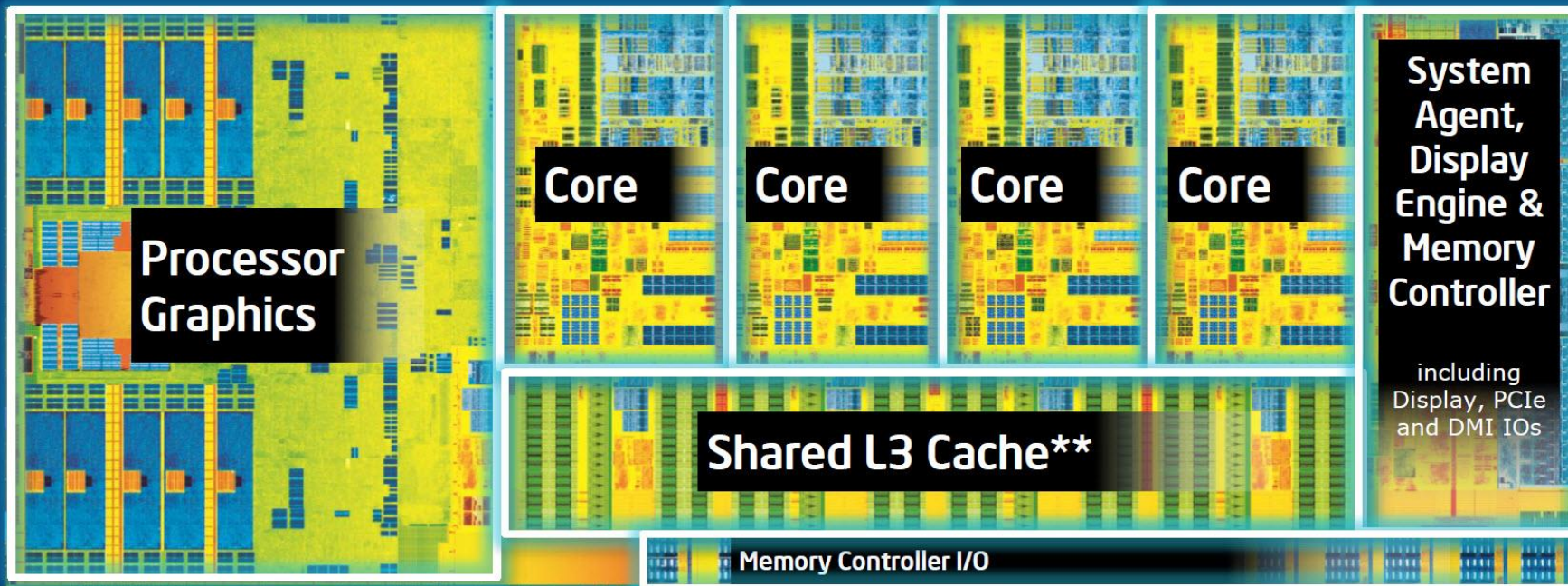
Feature	Nehalem	Sandy Bridge
Load Buffers	48	64
Store Buffers	32	36
Scheduler Entries	36	54
Integer Register File	N/A	160
Floating Point Register File	N/A	144
ROB Entries	128	168



Intel Haswell MicroArchitecture



4th Generation Intel® Core™ Processor Die Map *22nm Tri-Gate 3-D Transistors*



Quad core die shown above

Transistor count: 1.4 Billion

Die size: 177mm²

** Cache is shared across all 4 cores and processor graphics



Intel Haswell MicroArchitecture

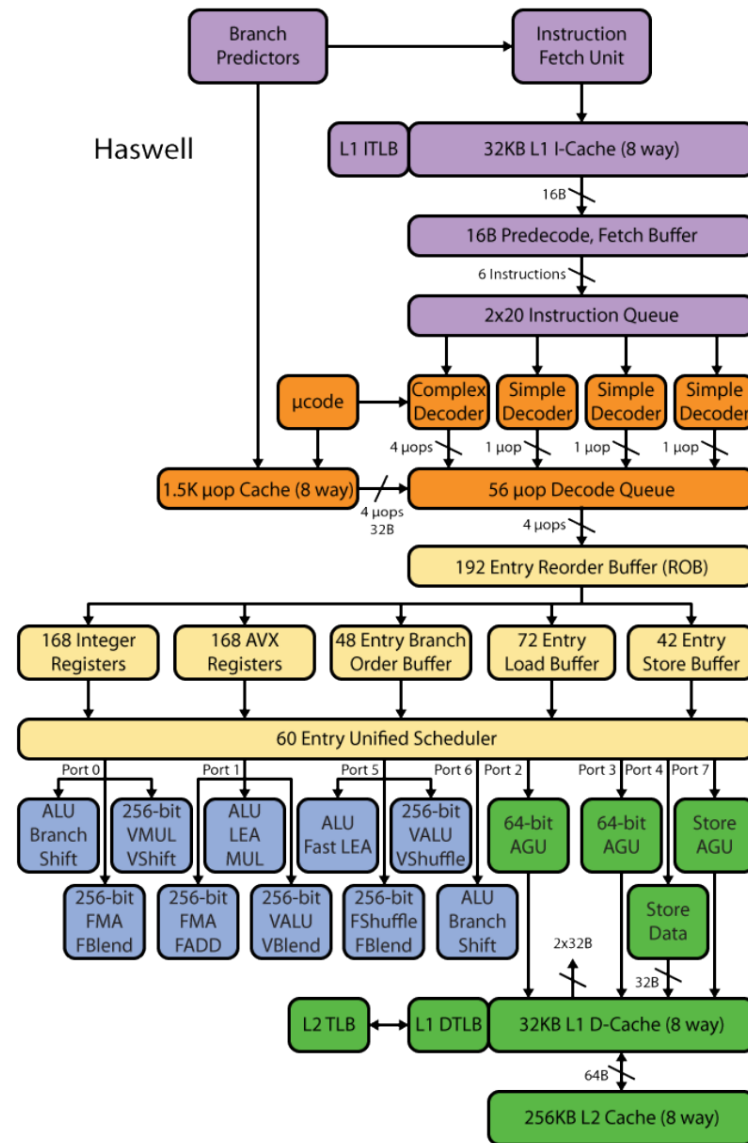
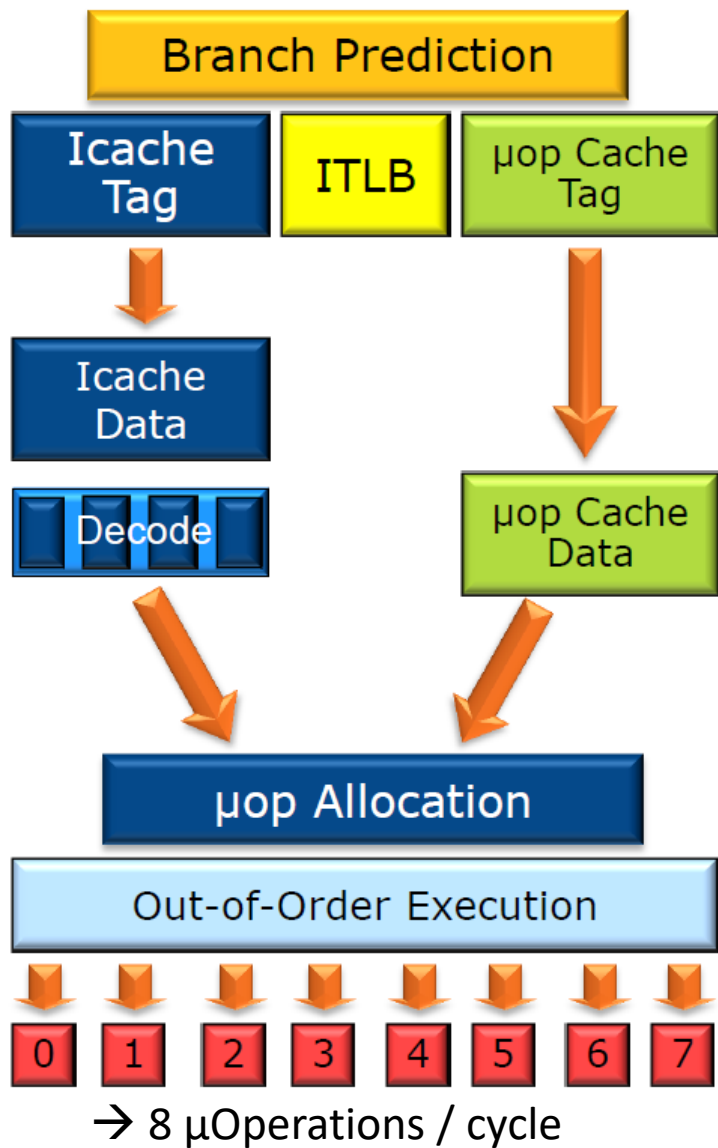


- More parallelism in every generation
- No pipeline growth – still 14 stages
- “Stacked” System on a Chip (SoC)
- Active idle – less power consumption, but instant resume
- New instructions – Advanced Vector Extension 2 (AVX2)

Feature	Nehalem	Sandy Bridge	Haswell
Out-of-Order window (ROB)	128	168	192
Load Buffers	48	64	72
Store Buffers	32	36	42
Scheduler Entries	36	54	60
Integer Register File	N/A	160	168
Floating Point Register File	N/A	144	168
Allocation Queue	28/thread	28/thread	56/thread



Intel Haswell MicroArchitecture

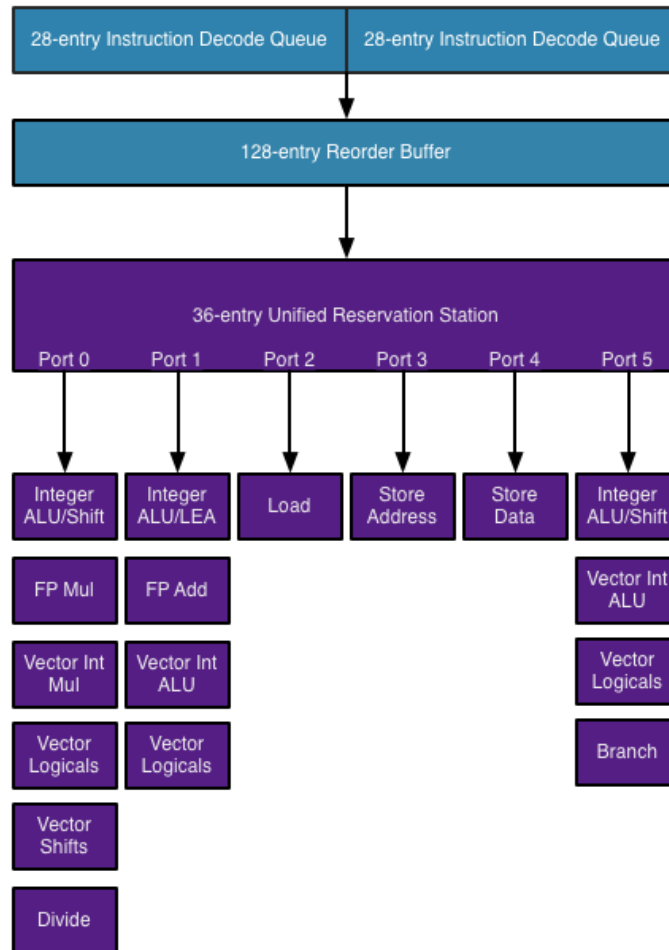




Execution Engine – Nehalem



Intel Nehalem Execution Engine

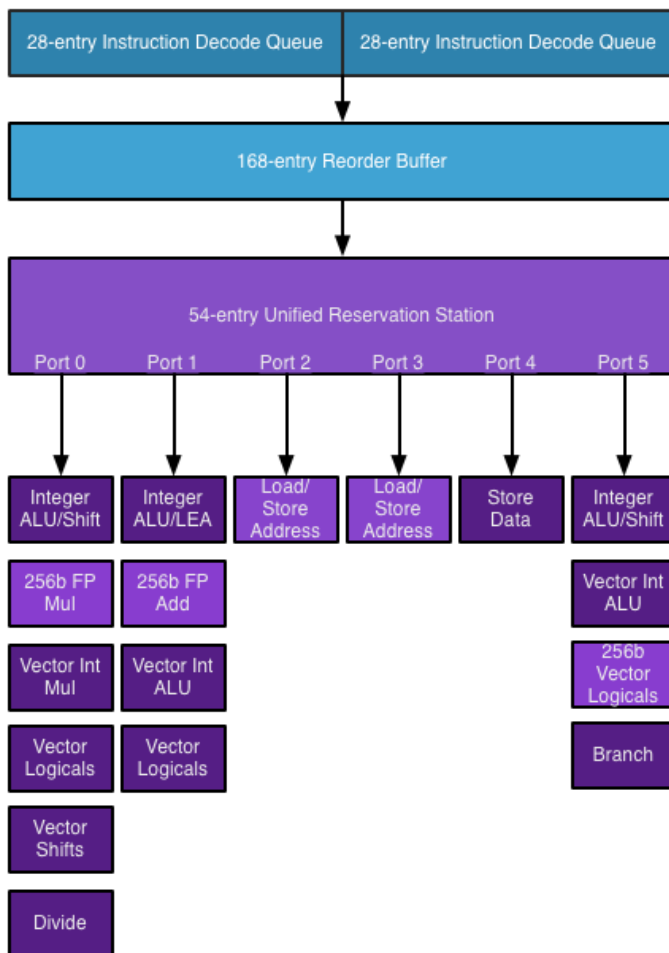




Execution Engine – Sandy Bridge



Intel Sandy Bridge Execution Engine

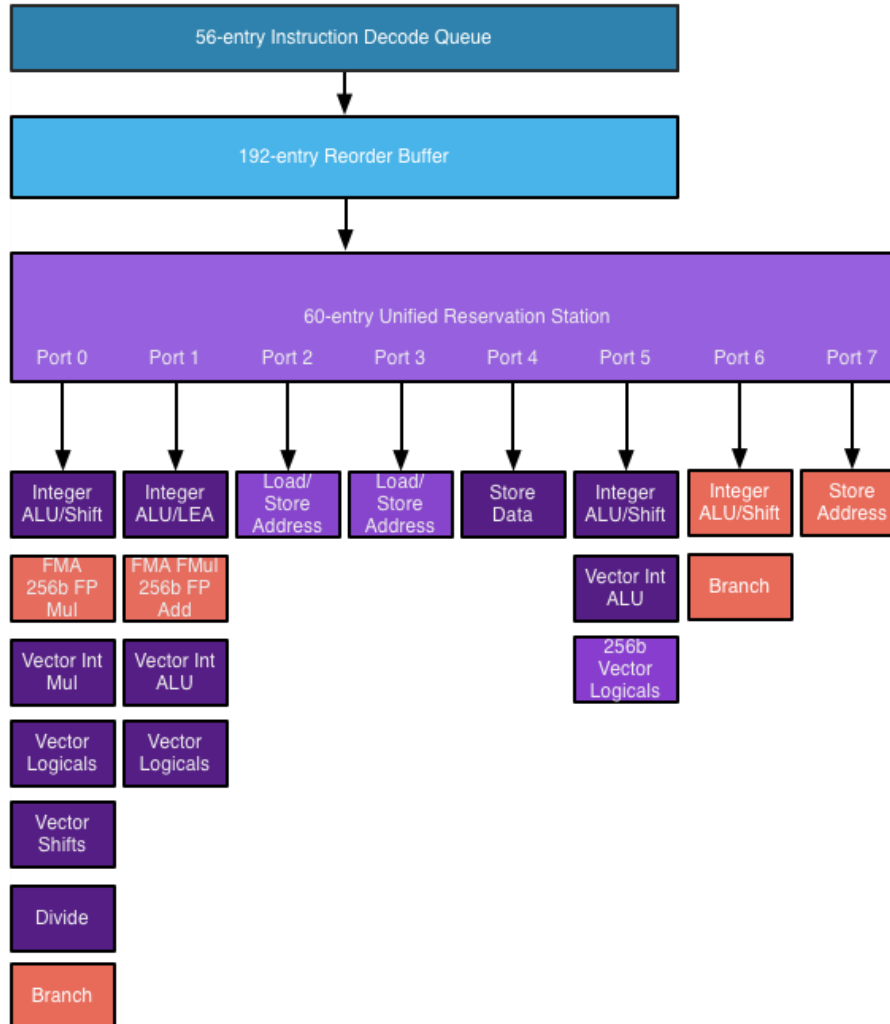




Execution Engine – Haswell



Intel Haswell Execution Engine





Intel Skylake MicroArchitecture



- More parallelism in every generation
- No pipeline growth – still 14 stages
- 4-way associative layer 2 cache!
- Improved Hyper-Threading performance
- Improved Branch Predictor – higher capacity, AVX2

Feature	Nehalem	Sandy Bridge	Haswell	Skylake
Out-of-Order window (ROB)	128	168	192	224
Load Buffers	48	64	72	72
Store Buffers	32	36	42	56
Scheduler Entries	36	54	60	97
Integer Register File	N/A	160	168	180
Floating Point Register File	N/A	144	168	168
Allocation Queue	28/thread	28/thread	56/thread	64/thread



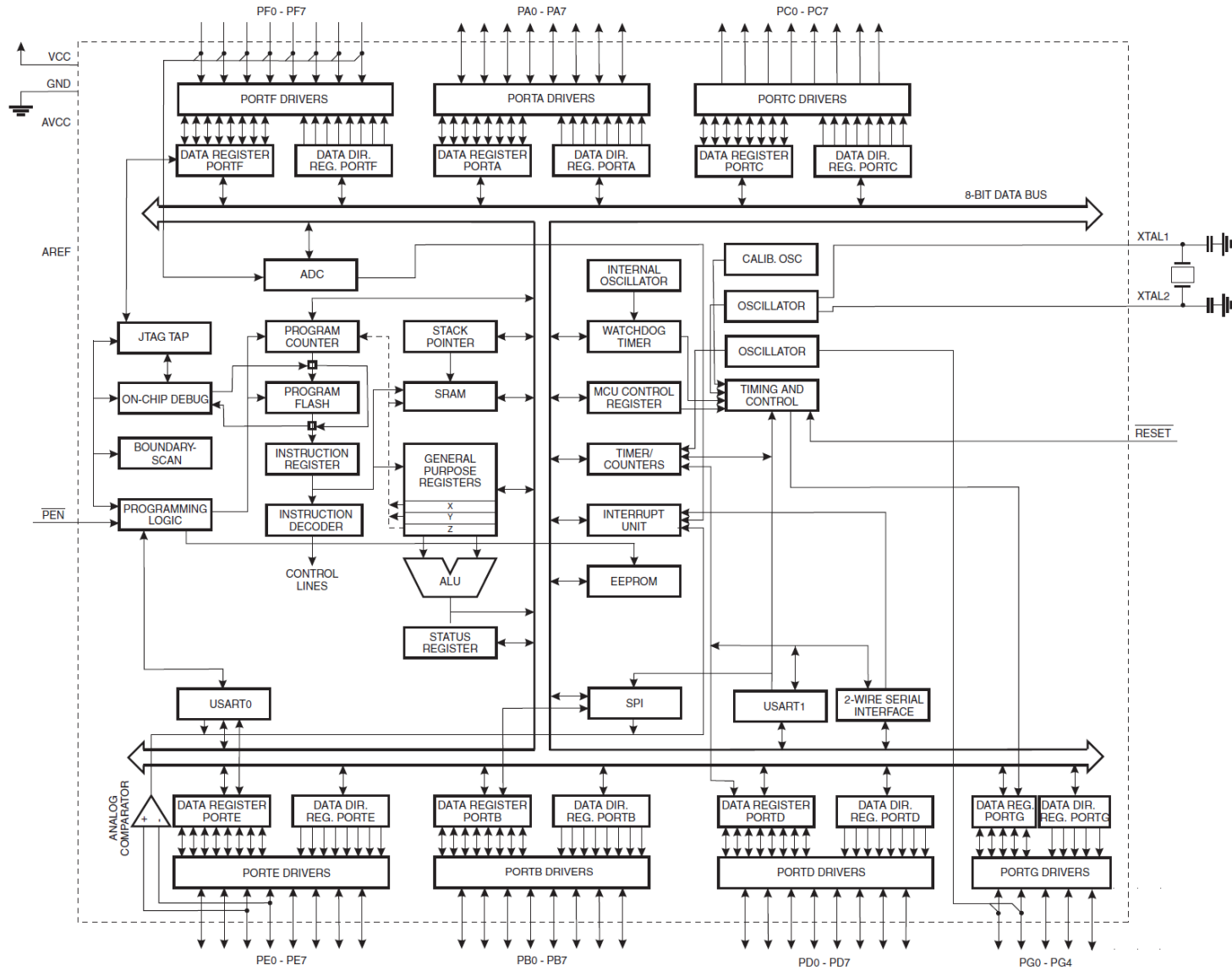
Other Architectures



- Micro-Controllers
- FPGAs
- SoC
- GPUs
-

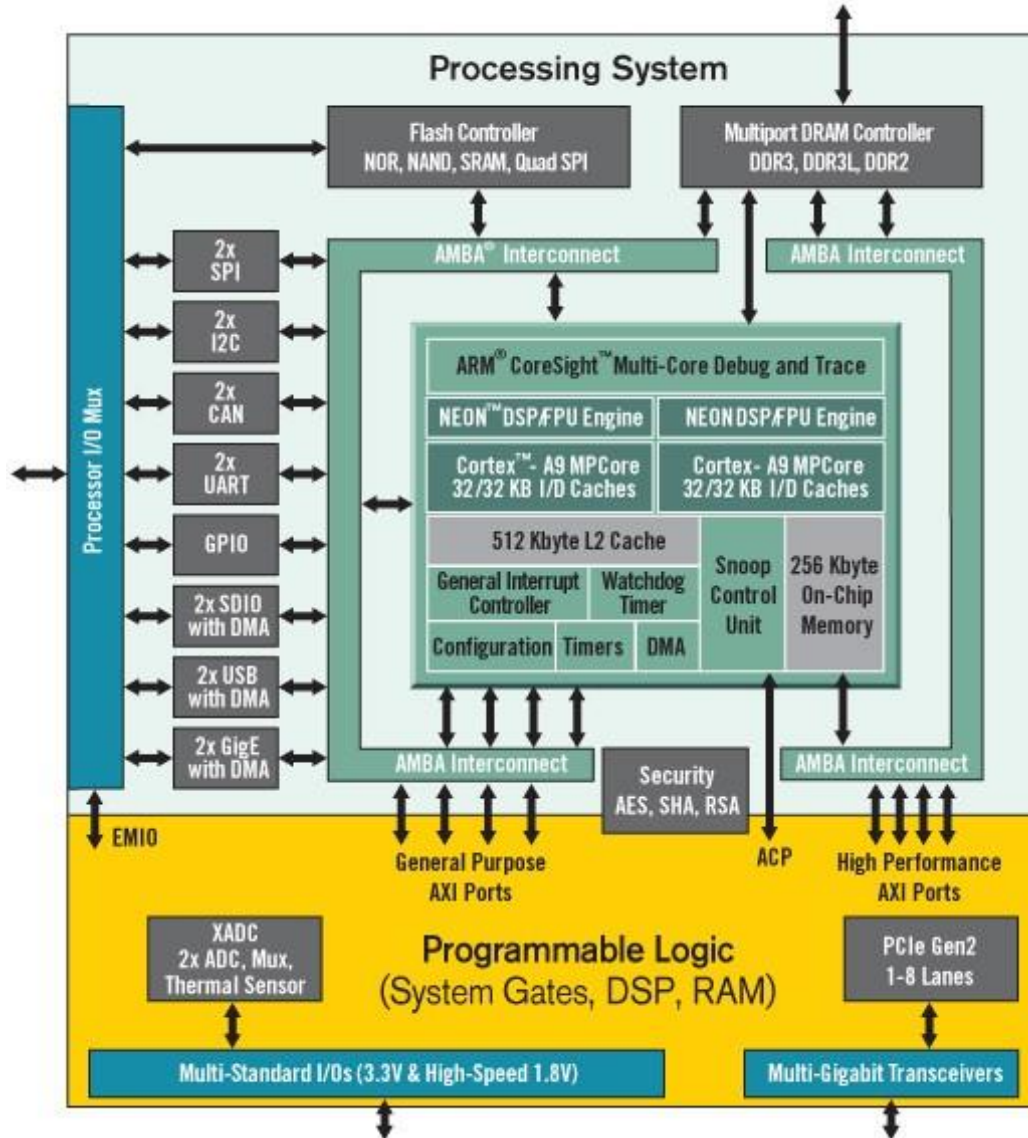


ATMEL ATmega 64 Micro-Controller





Xilinx ZYNQ – SoC





LEARN FOR THE EXAM!
IT'S NOT GOING TO BE EASY!



References



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