A1. (1.5 p) Design a 32-bit ALU for the following operations: ADD, SUB, INC, DEC, SLT. Design the 1-bit ALU by using only one adder and the minimum number of components and control signals. Extend the 1-bit ALU to obtain the 32-bit ALU. Show the schematic with control signals and a table with the control signal values for the required operations.

A2. (1.5 p) For the following equation: x = a*b*c + d*(d – a); write the corresponding instructions for 0, 1, 2 and 3 (load/store) address machines. a, b, c and d are in memory cells that must not be modified and x must be written in memory.

A3. (2.0 p) Define a SWAP (exchange the contents of two registers) instruction for the Single-Cycle and Multi-Cycle CPUs. Define the instruction format. Write the RTL Abstract and Concrete for this new instruction. Draw the complete data-paths highlighting the needed modifications. Present the values of the control signals for the new instruction.

A4. (2.5 p) Implement the JAL instruction in MIPS Pipeline. Draw the complete data-path, highlight the needed modifications. Present the values of the control signals for the JAL instruction.

A5. (1.0 p) A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clk cycles): Integer Unit – 1, FP Add – 2, FP MUL – 10, FP DIV – 40. Identify the hazards and trace the following instructions using the Tomasulo Algorithm (draw the table):
LD F6, R2; ADDD F6, F8, F2; MULD F1, F6, F2; ADDD F1, F3, F2; DIVD F8, F1, F6; ADDD F6, F8, F2; ADDD F2, F3, F2;

A6. (1.5 p) A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 512 KB cache memory for this CPU. The block size is 64 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 2-way set associative cache memory.

B1. (1.5 p) Describe the Booth multiplication method. Show the data path, ASM diagram and trace an example.

B2. (1.5 p) For the following equation: $w = a \cdot x^3 - b \cdot x^2 + c \cdot x - d$ draw the DFG without constraints and the DFG with 1 Adder/Subtractor and 1 Multiplier. Using HLS, design a circuit that implements the equation with the before mentioned constraints. Draw the data-path of the circuit highlighting the control signals. Write the RTL Concrete statements and present a table with the control signals values.

B3. (2.0 p) Modify the Single-Cycle and Multi-Cycle CPUs for the JALR (jump and link register) instruction. Define the instruction format. Write the RTL Abstract and Concrete for this new instruction. Draw the data-paths highlighting the needed modifications. Present the control signals values for the new instruction.

B4. (2.5 p) Design a Micro-Programmed Control Unit for the 2-Bus MIPS Architecture for MIPS-lite instructions. Draw the data-path of the 2-Bus MIPS with control signals, write the RTL Abstract and Concrete for the MIPS-lite instructions and show the values of the control signals. Draw and **explain** the Micro-Programmed control unit.

B5. (1.0 p) A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clk cycles): Integer Unit – 1, FP Add – 2, FP MUL – 10, FP DIV – 40. Identify the hazards and trace the following instructions using the Scoreboard Algorithm (draw the table):
LD F6, R2; ADDD F6, F8, F2; MULD F1, F6, F2; ADDD F1, F3, F2; DIVD F8, F1, F6; ADDD F6, F8, F2; ADDD F2, F3, F2;

B6. (1.5 p) A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 256 KB cache memory for this CPU. The block size is 32 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 4-way set associative cache memory.