A1. (1.5 p) Define the Reorder Buffer Concept. What it is, what it is used for, how does it work.
A2. (1.5 p) Draw the pipeline diagram with and without forwarding for the following code sequence: lw $5, 100($7); sub $7, $5, $3; or $7, $6, $6; add $5, $5, $2; sw $8, 10($5). Identify and explain the hazards in the code sequence. How many clock cycles does it take to execute the code (in both configurations)?
A3. (2.0 p) Define a BMI (Block Memory Initialization) instruction for the 2-bus MIPS CPU. Define the instruction format (start address, block size and initialization value). Write the RTL Abstract and Concrete for this new instruction. Draw the complete data-path highlighting the needed modifications. Present the values of the control signals for the new instruction.
A4. (2.5 p) Implement the BGEZ instruction in MIPS Pipeline. Draw the complete data-path, highlight the needed modifications. Present the values of the control signals for the BGEZ instruction.
A5. (1.0 p) A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clk cycles): Integer Unit – 1, FP Add – 4, FP MUL – 7, FP DIV – 24. Identify the hazards and trace the following instructions using the **Tomasulo** Algorithm (draw the table):
LD F6, 12(R2); LD F2, 16(R3); ADDD F0, F2, F4; DIVD F10, F0, F6; SUBD F8, F6, F2; ADDI R2, R2, 8; ADDI R3, R3, 16; ADDD F6, F8, F2
A6. (1.5 p) A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 32KB cache memory for this CPU. The block size is 16 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 2-way set associative cache memory.

B1. (1.5 p) Compare the bimodal and local branch predictors. Draw the schematics and **explain** the difference between the two predictors.
B2. (1.5 p) Draw the pipeline diagram with and without forwarding for the following code sequence: lw $6, 40($7); add $8, $6, $3; or $1, $6, $6; add $8, $3, $2; sw $8, 20($1). Identify and explain the hazards in the code sequence. How many clock cycles does it take to execute the code (in both configurations)?
B3. (2.0 p) Define a MBFMR (Move Block from Memory to Register) instruction for the 1-bus MIPS CPU. Define the instruction format (start address, block size and destination register). Write the RTL Abstract and Concrete for this new instruction. Draw the complete data-path highlighting the needed modifications. Present the values of the control signals for the new instruction.
B4. (2.5 p) Implement the BLTZ instruction in MIPS Pipeline. Draw the complete data-path, highlight the needed modifications. Present the values of the control signals for the BLTZ instruction.
B5. (1.0 p) A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clk cycles): Integer Unit – 1, FP Add – 4, FP MUL – 7, FP DIV – 23. Identify the hazards and trace the following instructions using the **Scoreboard** Algorithm (draw the table):
LD F6, 12(R2); LD F2, 16(R3); ADDD F0, F2, F4; DIVD F10, F0, F6; SUBD F8, F6, F2; ADDI R2, R2, 8; ADDI R3, R3, 16; ADDD F6, F8, F2
B6. (1.5 p) A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 64 KB cache memory for this CPU. The block size is 64 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 4-way set associative cache memory.