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A2. (1.5 p) Describe the Register File's requirements for single-cycle, mux-based multi-cycle, 1, 2 and 3 bus architectures.

A3. (2.0 p) Modify the Single-Cycle and Multi-Cycle CPUs for the BGEZ (Branch on greater than or equal to zero) instruction. Define the instruction format. Write the RTL Abstract and Concrete for this new instruction. Draw the data-paths highlighting the needed modifications. Present the control signals values for the new instruction.

A4. (2.5 p) Implement the JR (jump register) instruction in MIPS Pipeline. Draw the complete data-path, highlight the needed modifications. Present the values of the control signals for the JR instruction.

A5. (1.0 p) Describe the BTB (Branch Target Buffer) concept. What it is, what it is used for, how does it work.

A6. (1.5 p) A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 128 KB cache memory for this CPU. The block size is 16 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 2-way set associative cache memory.

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B1. (1.5 p) Design a 16-bit ALU for ADD, SUB, INC and DEC, for 16-bit operands or 2 x 8-bit operands (MMX style). Draw the schematic with control signals using two 8-bit adders and the necessary auxiliary circuits. Show a table with the values of the control signals for the required operations.
B2. (1.5 p) Describe the hazards that may appear in MIPS pipeline together with the solutions for solving these hazards.
B3. (2.0 p) Modify the Single-Cycle and Multi-Cycle CPUs for the JAL (jump and link) instruction. Define the instruction format. Write the RTL Abstract and Concrete for this new instruction. Draw the data-paths highlighting the needed modifications. Present the control signals values for the new instruction.
B4. (2.5 p) Implement the BGTZ (Branch on greater than zero) instruction in MIPS Pipeline. Draw the complete data-path, highlight the needed modifications. Present the values of the control signals for the BGTZ instruction.
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