A1. (1.5 p) Design a 32-bit ALU for the following operations: ADD, SUB, INC, DEC, SLT. Design the 1-bit ALU by using only one adder and the minimum number of components and control signals. Extend the 1-bit ALU to obtain the 32-bit ALU. Show the schematic with control signals and a table with the control signal values for the required operations.

A2. (1.5 p) Design a circuit that implements the following equation: $y = 3 \cdot a + 4 \cdot b + c / 2$ using HLS with only one ALU (no multiplier or divider units are available). Draw the DFG and design a 1-bus data-path for this equation. Highlight the control signals and present a table with the control signals values.

A3. (2.0 p) Draw the data-path for the Single-Cycle CPU for implementing the following instructions: JAL, BGTZ and SLLV. Highlight the needed modifications. Define the instruction formats, write the RTL Abstract for all the required instructions. Show the control signals and their values for implementing the required instructions.

A4. (2.5 p) Design a Sequence/Jump Counter Control Unit for the 3-Bus MIPS Architecture for MIPS-lite instructions. Draw the data-path of the 3-Bus MIPS with control signals, write the RTL Abstract and Concrete for the MIPS-lite instructions. Show the values of the control signals as well as the sequencing mechanism for each instruction. Draw the Sequence/Jump Counter Control Unit. Explain your design.

A5. (1.5 p) Define a SWAPM instruction for MIPS pipeline (exchange the contents of a register with a memory location). Define the instruction format. Draw the pipeline data-path highlighting the needed modifications. Write the RTL Abstract and Concrete for this new instruction. Present the control signal values for the new instruction.

A6. (1.0 p) Compare the BTB and TLB concepts. What do these concepts represent, what are they used for, how do they work.

B1. (1.5 p) Design a 16-bit ALU for ADD, SUB, INC and DEC, for 16-bit operands or 2 x 8-bit operands (MMX style). Draw the schematic with control signals using two 8-bit adders and the necessary auxiliary circuits. Show a table with the values of the control signals for the required operations.

B2. (1.5 p) Design a circuit that implements the following equation: $y = 5 \cdot a - b / 8 + c - 2$ using HLS with only one ALU (no multiplier or divider units are available). Draw the DFG and design a 1-bus data-path for this equation. Highlight the control signals and present a table with the control signals values.

B3. (2.0 p) Draw the data-path for the Single-Cycle CPU for implementing the following instructions: JR, BGTZAL and SLTIU. Highlight the needed modifications. Define the instruction formats, write the RTL Abstract for all the required instructions. Show the control signals and their values for implementing the required instructions.

B4. (2.5 p) Design a Micro-Programmed Control Unit for the 2-Bus MIPS Architecture for MIPS-lite instructions. Draw the data-path of the 2-Bus MIPS with control signals, write the RTL Abstract and Concrete for the MIPS-lite instructions. Show the contents of the Microcode Memory (all control signals). Draw the Micro-Programmed control unit and explain the sequencing mechanism.

B5. (1.5 p) Define a SWAP instruction for MIPS pipeline (exchange the contents of two registers). Define the instruction format. Draw the pipeline data-path highlighting the needed modifications. Write the RTL Abstract and Concrete for this new instruction. Present the control signal values for the new instruction.

B6. (1.0 p) Compare the Local and Global Branch Prediction schemes. Draw the architectures of the 2 predictors and explain the differences between them.