

- A1. (1.5 p)** Design a 32-bit ALU for the following operations: ADD, SUB, INC, DEC, SLT, AND, OR, NAND, NOR. Design the 1-bit ALU by using only one adder and the minimum number of components and control signals. Explain how each operation is performed. Extend the 1-bit ALU to obtain the 32-bit ALU. Show the schematic with control signals and a table with the control signal values for the required operations.
- A2. (1.5 p)** Draw the pipeline diagram with and without forwarding for the following code sequence: Loop: LW r1, 200(r3); ORI r2, r1, 200; ADD r8, r1, r2; SUB r3, r8, r1; BEQ r3, r8, Loop. The Branches are resolved in the ID stage. Consider that the BEQ instruction is executed (the loop runs 2 times). Identify the hazards in the code sequence and explain each delay introduced for resolving the hazards.
- A3. (2.0 p)** Draw the complete data-path for the Single-Cycle CPU (all other instructions must work) for implementing the following instructions: SLTIU, SLL, BLTZAL. Highlight the needed modifications. Define the instruction formats, write the RTL Abstract for all the required instructions. Show the control signals and their values for implementing the required instructions.
- A4. (2.5 p)** Design a Micro-Programmed Control Unit for the 2-Bus MIPS Architecture for the Block Copy Instruction (copies a block of memory from source to destination). Define the instruction format; draw the data-path of the 2-bus MIPS with control signals for implementing this instruction; write the RTL Abstract and Concrete codes for this instruction. Show the values of the control signals; the contents of the Microcode Memory (only for this instruction); draw the Micro-Programmed control unit and explain the sequencing mechanism.
- A5. (1.5 p)** Define a BGEZAL instruction for MIPS pipeline. Define the instruction format. Draw the pipeline data-path highlighting the needed modifications. Write the RTL Abstract and Concrete for this new instruction. Present the control signal values for the new instruction (in each pipeline stage).
- A6. (1.0 p)** A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 4 MB cache memory for this CPU. The block size is 32 KB. Show the block diagram, and the address decoding for a direct mapped cache memory and a 4-way set associative cache memory.

- B1. (1.5 p)** Describe the Booth multiplication method. Draw the data-path of this multiplication method, the ASM diagram and give two numerical examples (multiply two 4-bit numbers, both signed and unsigned).
- B2. (1.5 p)** Draw the pipeline diagram with and without forwarding for the following code sequence: Loop: LW r1, 200(r3); ORI r2, r1, 200; ADD r8, r1, r2; SUB r3, r8, r1; BEQ r3, r8, Loop. The Branches are resolved in the MEM stage. Consider that the BEQ instruction is executed (the loop runs 2 times). Identify the hazards in the code sequence and explain each delay introduced for resolving the hazards.
- B3. (2.0 p)** Extend the Single-Cycle CPU ISA with the PUSH and POP Instructions. Draw the complete data-path for the Single-Cycle CPU (all other instructions must work) and highlight the needed modifications. Define the instruction formats, write the RTL Abstract for these new instructions. Show the control signals and their values for implementing the required instructions.
- B4. (2.5 p)** Design a Sequence/Jump Counter Control Unit for the 3-Bus MIPS for the Block Register Copy Instruction (copies a block of registers from the register file to memory). Define the instruction format; draw the data-path of the 3-bus MIPS with control signals for implementing this instruction; write the RTL Abstract and Concrete codes for this instruction. Show the values of the control signals; draw the Sequence/Jump Counter Control Unit and explain the sequencing mechanism.
- B5. (1.5 p)** Define a SLTIAL instruction for MIPS pipeline. Define the instruction format. Draw the pipeline data-path highlighting the needed modifications. Write the RTL Abstract and Concrete for this new instruction. Present the control signal values for the new instruction (in each pipeline stage).
- B6. (1.0 p)** A 32-bit CPU generates 32-bit addresses for a byte addressable memory Design a 2 MB cache memory for this CPU. The block size is 64 KB. Show the block diagram, and the address decoding for a direct mapped cache memory and a 4-way set associative cache memory.