A1. (1.5 p) Design a 32-bit ALU for the following operations: ADD, SUB, INC, DEC, AND, OR, SLT. Design the 1-bit ALU by using only one adder and the minimum number of components and control signals. Extend the 1-bit ALU to obtain the 32-bit ALU. Show the schematic with control signals and a table with the control signal values for the required operations.

A2. (1.5 p) Describe the Register File's requirements for single-cycle, mux-based multi-cycle, 1, 2 and 3 bus architectures and pipeline.

A3. (2.0 p) Modify the Single-Cycle and Multi-Cycle CPUs for the BGEZAL instruction. Define the instruction format. Write the RTL Abstract and Concrete for this new instruction. Draw the data-paths highlighting the needed modifications. Present the control signals values for the new instruction.

A4. (2.5 p) Define a Block Copy instruction for 2-bus based MIPS Architecture (copies a block of memory from source to destination). Define the instruction format (source and destination addresses, block size).Draw the 2-bus based MIPS data-path with control signals, highlighting the needed modifications. Write the RTL abstract and concrete for a Block Copy instruction. Design a Micro-Programmed Control Unit only for this instruction. Explain the sequencing mechanism.

A5. (1.5 p) Implement the JAL instruction in MIPS Pipeline. Draw the complete data-path, highlighting the needed modifications. Present the values of the control signals for the JAL instruction.

A6. (1.0 p) Explain the following concepts: Speculative Execution, Reorder Buffer. What do these concepts represent, what are they used for, how do they work.