CA Exam, 08.06.2018 – English, R1 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions in order. The answers must occupy maximum 2 lines on the exam sheet. **(4.0 p)**

1. What is CISC?
2. What does MIPS mean?
3. What is the difference between ASAP and ALAP?
4. What are the execution phases of an instruction?
5. What is PC absolute addressing? Is it used in MIPS?
6. What is the function field (from instruction format) used for?
7. What is overflow, when can it happen?
8. How many memories are used in the single-cycle MIPS processor?
9. Give an example of µInstruction encoding.
10. What is a structural hazard?
11. What is WAW hazard? Can it appear in 5 stage pipeline MIPS?
12. What is the purpose of the CDB (common data bus2) in Tomasulo?
13. What is speculation / speculative instruction execution?
14. Do the instructions in a speculative Tomasulo Architecture commit in order?
15. What is a PHT (global branch prediction)? Where does its address come from?
16. What is SMT (Simultaneous Multithreading)?
17. How is the data organized in a cache memory?
18. What is the Write-Through write policy in the cache?
19. What is a page fault?
20. What is a BTB (branch prediction)?

II. Draw the pipeline diagram with and without forwarding for the following code sequence: **lw $6, 40($7); add $8, $6, $3; or $1, $6, $6; add $8, $3, $2; sw $8, 20($1)**. Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence in the two configurations. **(1.5 p)**

III. Define a **BMI (block memory initialization)** instruction for **2-bus based MIPS Architecture** (initializes a block of memory with a predefined value from a register). Define the instruction format (memory addresses, block size, initialization value). Draw the 2-bus based MIPS data-path with control signals, highlighting the needed modifications. Write the RTL abstract and concrete for the **BMI** instruction. Design a Micro-Programmed Control Unit for the 2-bus based MIPS Architecture. Draw the Micro-Programed control unit. Show the values of the control signals as well as the sequencing mechanism only for the **BMI** instruction. Explain your design. **(2.5 p)**

IV. A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clock cycles): Integer Unit – 1, FP Add – 4, FP MUL – 7, FP DIV – 23. Identify the hazards and trace the following instructions using the **Scoreboard Algorithm** (draw the table):
LD F6, 12(R2); **LD** F2, 16(R3); **ADDD** F0, F2, F4; **DIVD** F10, F0, F6; **SUBD** F8, F6, F2; **ADDI** R2, R2, 8; **ADDI** R3, R3, 16; **ADDD** F6, F8, F2 **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 256 KB cache memory for this CPU. The block size is 32 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 4-way set associative cache memory. **(1.0 p)**

CA Exam, 08.06.2018 – English, R2 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions in order. The answers must occupy maximum 2 lines on the exam sheet. **(4.0 p)**

1. What is RISC?
2. What is the difference between a 2 address machine and a 3 address machine?
3. What is the idea of Booth's multiplication algorithm?
4. What does baud rate mean?
5. What is PC relative addressing? Give an example from MIPS.
6. How many memories are used in the multi-cycle MIPS processor?
7. Write RTL abstract for the following instruction: beq.
8. What is WAR hazard? Can it appear in 5 stage pipeline MIPS?
9. Who is responsible for filling the branch delay slot?
10. What is a µProgram / µCode Memory?
11. What is ILP (instruction level parallelism)?
12. What is forwarding and how is it implemented in the MIPS pipeline?
13. Do the instructions in a Scoreboard commit in order?
14. What happens in a Scoreboard when a hazard is detected?
15. What is a ROB (reorder buffer)?
16. What is a BHT (bimodal branch prediction)? Where does its address come from?
17. What is the write buffer for cache memories?
18. What is a TLB (virtual memory)?
19. What is a super-scalar architecture?
20. How is the data organized in a virtual memory?

II. Design a 16-bit ALU for **ADD, SUB, INC and DEC**, for 16-bit operands or 2 x 8-bit operands (MMX style). Draw the schematic with control signals using two 8-bit adders and the necessary auxiliary circuits. Show a table with the values of the control signals for the required operations. **(1.5 p)**

III. Define a **RFBI** (register file block initialization) instruction for the Mux-Based Multi-Cycle MIPS Architecture (initializes a block of registers with a predefined value). Define the instruction format (register value, source address, block size). Draw the Mux-Based Multi-Cycle MIPS data-path with control signals, highlighting the needed modifications. Write the RTL abstract and concrete for the **RFBI** instruction. Design a Sequence/Jump Counter Control Unit for Mux-based Multi-Cycle MIPS. Draw the Sequence/Jump Counter Control Unit. Show the values of the control signals as well as the sequencing mechanism only for the **RFBI** instruction. Explain your design. **(2.5 p)**

IV. A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clock cycles): Integer Unit – 1, FP Add – 4, FP MUL – 7, FP DIV – 24. Identify the hazards and trace the following instructions using the **Tomasulo Algorithm** (draw the table):
LD F6, 12(R2); LD F2, 16(R3); ADDD F0, F2, F4; DIVD F10, F0, F6; SUBD F8, F6, F2; ADDI R2, R2, 8; ADDI R3, R3, 16; ADDD F6, F8, F2 **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 64 KB cache memory for this CPU. The block size is 16 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 2-way set associative cache memory. **(1.0 p)**