CA Exam, 08.07.2018 – English **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions in order. The answers must occupy maximum 2 lines on the exam sheet. **(4.0 p)**

1. What does baud rate mean?
2. What is the UART frame format?
3. What is PC absolute addressing? Is it used in MIPS?
4. What is the "sa" field (from instruction format) used for?
5. Write RTL abstract for the following instruction: jal.
6. Write RTL abstract for the following instruction: sll.
7. How many registers are in the MIPS Register File?
8. Who is responsible for filling the branch delay slot?
9. What is a ROB (reorder buffer)?
10. Give an example of a RAW data hazard.
11. Give an example of µInstruction encoding.
12. How is the SLT operation implemented in an ALU?
13. What is the binary number representation used in today processors? 1's or 2's complement? Why?
14. What is register renaming?
15. What is speculation / speculative instruction execution?
16. What is the Write-Back write policy in the cache?
17. What is a BHT (bimodal branch prediction)? Where does its address come from?
18. What is a TLB (virtual memory)?
19. What is temporal locality (caches)?
20. What is AMAT?

II. Design a 16-bit ALU for **ADD, SUB, INC and DEC**, for 16-bit operands or 2 x 8-bit operands (MMX style). Draw the schematic with control signals using two 8-bit adders and the necessary auxiliary circuits. Show a table with the values of the control signals for the required operations. **(1.5 p)**

III. Define a **Store+** instruction (store with post-incremented addressing – the source register is incremented after the operation) for the pipeline MIPS CPUs. Define the instruction format. Draw the data-path with control signals, highlighting the needed modifications (the normal / usual instructions must work). Write the RTL Abstract and Concrete for this new instruction. Present the control signals values for the new instruction. **(2.0 p)**

IV. Modify the Single-Cycle and Multi-Cycle CPUs for the JAL (jump and link) instruction. Define the instruction format. Write the RTL Abstract and Concrete for this new instruction. Draw the data-paths highlighting the needed modifications (the normal / usual instructions must work). Present the control signals values for the new instruction. **(1.5 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 1MB cache memory for this CPU. The block size is 64 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 4-way set associative cache memory. **(1.0 p)**