CA Exam, 04.09.2018 – English **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions in order. The answers must occupy maximum 2 lines on the exam sheet. **(4.0 p)**

1. How many memories are used in the single-cycle MIPS processor?
2. What is a pipeline flush?
3. What is PC absolute addressing? Is it used in MIPS?
4. What is the "function" field (from instruction format) used for?
5. Write RTL abstract for the following instruction: jr.
6. Write RTL abstract for the following instruction: sllv.
7. How many registers are in the MIPS Register File?
8. Who is responsible for filling the branch delay slot?
9. What is a control hazard?
10. Give an example of a RAW data hazard.
11. Give an example of µInstruction encoding.
12. How is the SLT operation implemented in an ALU?
13. What is the binary number representation used in today processors? 1's or 2's complement? Why?
14. What is register renaming?
15. What is a 2-bit predictor (branch prediction)?
16. What is a cache memory?
17. What is AMAT?
18. What is a BHT (bimodal branch prediction)? Where does its address come from?
19. What is a TLB (virtual memory)?
20. What is temporal locality (caches)?

II. Using HLS, design a circuit that implements the following equation: r = x + y/16 + 4*z, with the following constraints: 1 ALU (There are no multiplication or division operations). Draw the data-path of the circuit. Highlight the control signals and present a table with the control signals values. **(1.0 p)**

III. Define a **BMI (block memory initialization)** instruction for the Mux-Based Multi-Cycle MIPS Architecture (initializes a block in memory with a predefined value). Define the instruction format (memory addresses, block size, initialization value). Draw the Mux-Based Multi-Cycle MIPS data-path with control signals, highlighting the needed modifications. Write the RTL abstract and concrete for the **BMI** instruction. Design a Micro-Programmed Control Unit for the Mux-based Multi-Cycle MIPS. Draw the Micro-Programed control unit with control signals. Show the values of the control signals as well as the sequencing mechanism only for the **BMI** instruction. Explain your design. **(2.5 p)**

IV. Modify the Single-Cycle and Multi-Cycle CPUs for the **JAL** (jump and link) instruction. Define the instruction format. Write the RTL Abstract and Concrete for this new instruction. Draw the data-paths highlighting the needed modifications (the normal / usual instructions must work). Present the control signals values for the new instruction. **(1.5 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 1MB cache memory for this CPU. The block size is 64 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 4-way set associative cache memory. **(1.0 p)**