CA Exam, 22.06.2019 – English, R1 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. Big endian: LSB byte at lower address. (T/F)	
2. The 0 address machine is called Register-Memory. (T/F)	
3. How many bits are needed for encoding a register's address in the MIPS instructions?	
4. How many memories are used in the pipeline MIPS processor?	
5. The 1 FF/state control unit uses a memory to generate the control signals. (T/F)	
6. How many clock cycles does a lw Instruction take in the multi-cycle MIPS processor?	
7. How many clock cycles does a beq Instruction take in the pipeline MIPS processor?	
8. Who is responsible for filling the branch delay slot in static branch prediction?	
9. Setting to 0 the write control signals for the RF and Data Memory is called pipeline ...	
10. WAW hazards can appear in 5 stage pipeline MIPS. (T/F)	
11. WAR hazards can appear in Speculative Tomasulo. (T/F)	
12. CDB conflict can never appear in Speculative Tomasulo. (T/F)	
13. Do the instructions in a Scoreboard commit in order?	
14. Who decides the ALU control for R-type instructions in MIPS?	
15. In the multi-cycle MIPS the branch address is computed in the ALU. (T/F)	
16. A BHT is a table of 2-bit predictors indexed by a subset of the lower PC bits. (T/F)	
17. The replacement policy for a page fault is „write back". (T/F)	
18. How many bits are needed to address a 4GB RAM?	
19. A TLB is a cache memory that stores virtual addresses. (T/F)	
20. How many clock cycles are necessary to execute 100 intructions in MIPS pipeline?	

(T/F) = True or False

II. Using HLS, design a circuit that implements the following equation: $w = a \cdot (b \cdot x + z) - c \cdot (a \cdot y + x)$ with the following constraints: 1 ALU and 1 Multiplier. Draw the data-path of the circuit with a mux based architecture. Write the RTL concrete, highlighting the values of the control signals. **(1.0 p)**

III. Define a **Load+ (load word with post increment)** instruction for the 3-bus based multi-cycle MIPS architecture. Define the instruction format. Draw the 3-bus based multi-cycle MIPS data-path with control signals, highlighting the needed modifications. Write the RTL abstract and concrete for the **Load+** instruction. Design a 1-FF/state control unit for the 3-bus based multi-cycle MIPS. Draw the 1-FF/state control unit with control signals. Show the values of the control signals as well as the sequencing mechanism only for the **Load+** instruction. Explain your design. **(2.5 p)**

IV. Modify the single-cycle and multi-cycle CPUs for the **JALR** (jump and link register) instruction. Define the instruction format. Write the RTL abstract and concrete for this new instruction. Draw the data-paths highlighting the needed modifications (the normal / usual instructions must work). Present the control signals values for the new instruction. **(1.5 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 512KB cache memory for this CPU. The block size is 64 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 4-way set associative cache memory. **(1.0 p)**

CA Exam, 22.06.2019 – English, R2 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. Little endian: LSB byte at lower address! (T/F)	
2. The 1 address machine is called accumulator. (T/F)	
3. A jmp instruction for MIPS can be used to jump anywhere in the instr. memory. (T/F)	
4. How many memories are used in the multi-cycle MIPS processor?	
5. How many bits are used for encoding the "sa" field in the MIPS instructions?	
6. The sllv instruction uses the „sa" field from the MIPS instruction. (T/F)	
7. How many clock cycles does a lw Instruction take in the pipeline MIPS processor?	
8. How many instructions enter in classic MIPS pipeline until a branch outcome is known?	
9. What is the logic gate used to implement a zero detector?	
10. RAW hazards can appear in 5 stage pipeline MIPS. (T/F)	
11. CDB conflict can never appear in the Scoreboard method. (T/F)	
12. Do the instructions in a Tomasulo Architecture commit in order?	
13. In the multi-cycle MIPS the branch address is computed in a separate adder. (T/F)	
14. On overflow an ... happens in MIPS.	
15. Where does the store information (addr + data) come from in Speculative Tomasulo?	
16. The micro-programmed control unit uses a PLA to generate the control signals. (T/F)	
17. What kind of data structure is used to form the write buffer for cache memories?	
18. A BTB is a cache memory that stores virtual addresses. (T/F)	
19. The execution of instructions before control dependences are resolved is called ...	
20. What is the size of the memory that has 20 address bits?	

(T/F) = True or False

II. Using HLS, design a circuit that implements the following equation: $r = a \cdot b \cdot c + d(d - a)$, with the following constraints: 1 ALU and 1 Multiplier. Draw the data-path of the circuit using a 1-bus architecture. Write the RTL concrete, highlighting the values of the control signals. **(1.0 p)**

III. Define a **SWAPM** instruction for the mux-based multi-cycle MIPS architecture (exchange the contents of a register with a memory location). Define the instruction format. Draw the mux-based multi-cycle MIPS data-path with control signals, highlighting the needed modifications. Write the RTL abstract and concrete for the **SWAPM** instruction. Design a micro-programmed control unit for the mux-based multi-cycle MIPS. Draw the micro-programed control unit with control signals. Show the values of the control signals as well as the sequencing mechanism only for the **SWAPM** instruction. Explain your design. **(2.5 p)**

IV. Modify the single-cycle and pipeline CPUs for the **BLTZ** instruction. Define the instruction format. Write the RTL abstract and concrete for this new instruction. Draw the data-paths highlighting the needed modifications (the normal / usual instructions must work). Present the control signals values for the new instruction. **(1.5 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 128KB cache memory for this CPU. The block size is 32 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 2-way set associative cache memory. **(1.0 p)**