CA Exam, 11.07.2019 – English, R1 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. Little endian: LSB byte at lower address! (T/F)	
2. The 0 address machine is called Stack. (T/F)	
3. How many bits are needed for encoding the "func" field in the MIPS instructions?	
4. How many memories are used in the single-cycle MIPS processor?	
5. What is the opcode value for R-type instructions?	
6. How many clock cycles does a lw Instruction take in the multi-cycle MIPS processor?	
7. How many clock cycles does a beq Instruction take in the pipeline MIPS processor?	
8. What is the logic gate used to implement a zero detector?	
9. Setting to 0 the write control signals for the RF and Data Memory is called pipeline ...	
10. RAR hazards can appear in 5 stage pipeline MIPS. (T/F)	
11. WAW hazard can appear in speculative Tomasulo. (T/F)	
12. A BHR is a shift register that stores last k branches. (T/F)	
13. The instructions in a Scoreboard commit in the order they were issued. (T/F)	
14. The instructions in Speculative Tomasulo commit in order. (T/F)	
15. In the multi-cycle MIPS the branch address is computed in the ALU. (T/F)	
16. A PHT is an array of 2-bit predictors. (T/F)	
17. A BTB is a cache memory that stores brach target addresses. (T/F)	
18. How many bits are needed to address a 4GB RAM?	
19. A TLB is a cache memory that stores physical page addresses . (T/F)	
20. How many clock cycles are necessary to execute 500 intructions in MIPS pipeline?	

(T/F) = True or False

II. Design a 32-bit ALU for the following operations: ADD, SUB, NAND, NOR, Pass A, Negate A, Decrement A. Design the 1-bit ALU by using a single adder circuit and then extend it in order to obtain the 32-bit ALU. Draw the schematic with control signals and present a table with the control signal values for the required operations. **(1.5 p)**

III. Implement the BNE, BLTZ and JAL instructions in the single-cycle and Mux-based multi-cycle MIPS CPUs. Draw the complete data-paths for the two MIPS architectures, highlighting the needed modifications. Write the RTL Abstract and RTL Concrete for these new instructions; show the control signals for each instructions. Explain your design. **(2.0 p)**

IV. A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clock cycles): Integer Unit – 1, FP Add – 4, FP MUL – 7, FP DIV – 23. Identify the hazards and trace the following instructions using the classic Tomasulo Algorithm (draw and fill the table): **LD F6, 12(R2); LD F2, 16(R3); ADDD F0, F2, F4; DIVD F10, F0, F6; SUBD F8, F6, F2; ADDI R2, R2, 8; ADDI R3, R3, 16; ADDD F6, F8, F2** **(1.0 p)**

V. Draw the pipeline diagram with and without forwarding for the following code sequence: **lw $6, 20($7); add $8, $6, $3; or $1, $6, $6; add $8, $3, $2; sw $8, 20($1)**. Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence in the two configurations. **(1.5 p)**