CA Exam, 03.09.2019 – English, R1 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. MIPS uses the PC relative addressing mode. (T/F)	
2. The 1 address machine is called Accumulator. (T/F)	
3. How many bits are needed for encoding the "sa" field in the MIPS instructions?	
4. How many registers does a MIPS register file have?	
5. What is the maximum number of instructions that can be encoded in MIPS?	
6. How many clock cycles does an addi Instruction take in the multi-cycle MIPS?	
7. How many clock cycles does an addi Instruction take in the pipeline MIPS?	
8. What is the logic gate used to implement a zero detector?	
9. Structural hazards can appear in 5 stage pipeline MIPS. (T/F)	
10. RAW hazards can appear in 5 stage pipeline MIPS. (T/F)	
11. WAW hazard can not appear in speculative Tomasulo. (T/F)	
12. The address for the BHT is a subset of the PC. (T/F)	
13. An architecture that dispatches more instructions / clock cycle is called ...	
14. The instructions in Speculative Tomasulo commit in order. (T/F)	
15. In the multi-cycle MIPS the branch address is computed in the ALU. (T/F)	
16. How is the data organized in the main memory? In ...	
17. A BTB is a cache memory that stores brach target addresses. (T/F)	
18. How many bits are needed to address a 1 GB RAM?	
19. How is the data organized in a cache memory? In ...	
20. How many clock cycles are necessary to execute 200 intructions in a MIPS pipeline?	

(T/F) = True or False

II. Design a 32-bit ALU for ADD, SUB, INC and DEC, for 32-bit operands, 2 x 16-bit operands or 4 x 8-bit operands (MMX style). Draw the schematic with control signals using **4 x 8-bit adders** and the necessary auxiliary circuits. Show a table with the values of the control signals for the required operations for all variants. **(1.5 p)**

III. Implement the SLT, JR and JAL instructions in the single-cycle and Mux-based multi-cycle MIPS CPUs. Draw the complete data-paths for the two MIPS architectures, highlighting the needed modifications. Write the RTL Abstract and RTL Concrete for these new instructions; show the control signals for each instructions. Explain your design. **(2.0 p)**

IV. A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clock cycles): Integer Unit – 1, FP Add – 4, FP MUL – 10, FP DIV – 40. Identify the hazards and trace the following instructions using the classic Tomasulo Algorithm (draw and fill the table): **LD F6, 12(R2); SD F6, 16(R3); MULD F1, F6, F2; ADDD F1, F5, F4; DIVD F8, F1, F6; ADDD F6, F8, F2; ADDD F1, F3, F2** **(1.0 p)**

V. Define a SWAP instruction for MIPS pipeline (exchange the contents of two registers). Define the instruction format. Draw the pipeline data-path highlighting the needed modifications. Write the RTL Abstract and Concrete for this new instruction. Present the control signal values for the new instruction. **(1.5 p)**