CA Exam, 03.06.2022 – English, R1 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. How many bits does one need to address a 8 MB RAM?	
2. The branch address in the single-cycle MIPS is computed in the ALU. (T/F)	
3. How is the data organized in a cache memory?	
4. How many bits are used for encoding the "func" field in the MIPS instructions?	
5. The Hardwired control unit uses a memory to generate the control signals. (T/F)	
6. The sll instruction uses the „sa" field from the MIPS instruction. (T/F)	
7. How many clock cycles does a beq Instruction take in the pipeline MIPS processor?	
8. How many clock cycles does a beq Instruction take in the multi-cycle MIPS processor?	
9. Setting to 0 the write control signals for the RF and Data Memory is called pipeline ...	
10. What is a reservation station in Tomasulo?	
11. CDB conflict can never appear in Speculative Tomasulo. (T/F)	
12. In the multi-cycle MIPS, the branch address is computed in a separate adder. (T/F)	
13. Do the instructions in a Scoreboard finish in order?	
14. A reorder buffer in Speculative Tomasulo is a stack of instructions. (T/F)	
15. The last step of Speculative Tomasulo is called ...	
16. A BHT is a table of 2-bit predictors indexed by a subset of the lower PC bits. (T/F)	
17. The replacement policy for a page fault is „write back". (T/F)	
18. A superscalar architecture dispatches only one instruction per cycle. (T/F)	
19. A TLB is a cache memory that stores virtual addresses. (T/F)	
20. How many clock cycles are necessary to execute 15 instructions in MIPS pipeline?	

(T/F) = True or False

II. Design a 32-bit ALU for the following operations: ADD, SUB, NAND, NOR, Pass A, Negate A, Decrement A. Design the 1-bit ALU by using only one adder and the minimum number of components and control signals. Explain how each operation is performed. Extend the 1-bit ALU to obtain the 32-bit ALU. Draw the schematic with control signals and present a table with the control signal values for the required operations. **(1.5 p)**

III. Modify the Single-cycle MIPS CPU for the following instructions: **Store+** (store with post increment), **BGETZAL** (Branch on greater than or equal to zero and link), JAL (jump and link). Define the instruction formats, write the RTL Abstract for all the required instructions. Draw the modified data-path. Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. Draw the pipeline diagram with and without forwarding for the following code sequence: **lw $6, 20($7); add $8, $6, $3; or $1, $6, $6; add $8, $3, $2; sw $8, 20($1).** Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence in the two configurations. **(1.0 p)**

V. A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clock cycles): Integer Unit – 1, FP Add – 4, FP MUL – 7, FP DIV – 23. Identify the hazards and trace the following instructions using the classic **Tomasulo** Algorithm (draw and fill the table): **LD F6, 12(R2); LD F2, 16(R3); ADDD F0, F2, F4; DIVD F10, F0, F6; SUBD F8, F6, F2; ADDI R2, R2, 8; ADDI R3, R3, 16; ADDD F6, F8, F2** **(1.0 p)**

CA Exam, 03.06.2022 – English, R2 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. How many bits does one need to address a 16 GB RAM?	
2. A jmp instruction for MIPS can be used to jump anywhere in the instr. memory. (T/F)	
3. How is the data organized in a virtual memory?	
4. How many bits are used for encoding the "sa" field in the MIPS instructions?	
5. The Microprogrammed control unit uses a memory to generate the control signals. (T/F)	
6. The sllv instruction uses the „sa" field from the MIPS instruction. (T/F)	
7. How many clock cycles does a sw Instruction take in the pipeline MIPS processor?	
8. How many clock cycles does a beq Instruction take in the single-cycle MIPS processor?	
9. What is the logic gate used to implement a zero detector?	
10. In the multi-cycle MIPS, the branch address is computed in the ALU. (T/F)	
11. CDB conflict can never appear in the Scoreboard method. (T/F)	
12. Do the instructions in a Speculative Tomasulo Architecture commit in order?	
13. WAR hazards can appear in Speculative Tomasulo. (T/F)	
14. Where does the store information (address + data) come from in Speculative Tomasulo?	
15. In Tomasulo the nb. of reservation stations equals the number of functional units. (T/F)	
16. A 2-bit predictor is implemented with a decoder. (T/F)	
17. What data structure is used to form the write buffer for cache memories?	
18. A BTB is a cache memory that stores virtual addresses. (T/F)	
19. The execution of instructions before control dependences are resolved is called ...	
20. How many clock cycles are necessary to execute 99 instructions in MIPS pipeline?	

(T/F) = True or False

II. Design a 32-bit ALU for the following operations: ADD, SUB, INC, DEC, SLT, AND, OR, NAND, NOR. Design the 1-bit ALU by using only one adder and the minimum number of components and control signals. Explain how each operation is performed. Extend the 1-bit ALU to obtain the 32-bit ALU. Show the schematic with control signals and a table with the control signal values for the required operations. **(1.5 p)**

III. Modify the Single-cycle MIPS CPU for the following instructions: **Load+** (load with post increment), **BGTZ** (Branch on greater than zero), **JALR** (jump and link register). Define the instruction formats, write the RTL Abstract for all the required instructions. Draw the modified data-path. Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. Draw the pipeline diagram **with** and **without** forwarding for the following code sequence: **lw $5, 100($7); sub $7, $5, $3; add $5, $5, $2; sw $7, 10($5); lw $7, 20($5).** Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence in the two configurations. **(1.0 p)**

V. A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clock cycles): Integer Unit – 1, FP Add – 4, FP MUL – 7, FP DIV – 23. Identify the hazards and trace the following instructions using the classic **Scoreboard** Algorithm (draw and fill the table): **LD F6, 12(R2); LD F2, 16(R3); ADDD F0, F2, F4; DIVD F10, F0, F6; SUBD F8, F6, F2; ADDI R2, R2, 8; ADDI R3, R3, 16; ADDD F6, F8, F2** **(1.0 p)**