CA Exam, 26.07.2022 – English **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. How many bits does one need to address a 32 MB RAM?	
2. How is the data organized in a cache memory?	
3. In the single-cycle MIPS, the branch address is computed in the ALU. (T/F)	
4. In the multi-cycle MIPS, the branch address is computed in the ALU. (T/F)	
5. The micro-programmed control unit uses a memory to store the control signals. (T/F)	
6. How many clock cycles does a sw instruction take in the single-cycle MIPS processor?	
7. How many clock cycles does a sw instruction take in the pipeline MIPS processor?	
8. How many clock cycles does a sw instruction take in the multi-cycle MIPS processor?	
9. Setting to 0 the write control signals for the RF and Data Memory is called pipeline ...	
10. Do the instructions in a Speculative Tomasulo Architecture commit in order?	
11. CDB conflict can never appear in Speculative Tomasulo. (T/F)	
12. A reorder buffer in Speculative Tomasulo is a stack of instructions. (T/F)	
13. The last step of Speculative Tomasulo is called ...	
14. What data structure is used to form the write buffer for cache memories?	
15. A TLB is a cache memory that stores virtual addresses. (T/F)	
16. A BTB is a table of 2-bit predictors indexed by a subset of the lower PC bits. (T/F)	
17. The replacement policy for a page fault is „write through”. (T/F)	
18. What is the logic gate used to implement the zero detector in the ALU?	
19. On overflow an ... happens in MIPS.	
20. An architecture that dispatches more instructions / clock cycle is called ...	

(T/F) = True or False

II. Design a 32-bit ALU for the following operations: ADD, SUB, NAND, NOR, Pass A, Negate A, Decrement A, for 32-bits operands, 2 x 16-bits operands, 4 x 8-bits operands (MMX style). Explain how each operation is performed. Draw the schematic with control signals using **four** (4) 8-bit adders and the necessary auxiliary circuits on 8-bits. Present a table with the control signal values for the required operations (for all 3 configurations). **(1.5 p)**

III. Modify the Single-cycle MIPS CPU for the following instructions: **Store+** (store with post increment addressing), **Load-** (load with post decrement addressing), **BLTZAL** (Branch on less than zero and link). Define the instruction formats, write the RTL Abstract for all the required instructions. Draw the modified data-path. Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. Implement the **JAL** instruction in MIPS Pipeline. Draw the complete data-path, highlighting the needed modifications. Present the values of the control signals for the JAL instruction. **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 512 KB cache memory for this CPU. The block size is 64 bytes. Show the block diagram, and the address decoding for a direct mapped cache memory and a 2-way set associative cache memory. **(1.0 p)**