CA Exam, 16.06.2023 – English, R1 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. Suppose the value 0x35 is loaded in RF[7]. What is the value in RF[7] after the execution of the following instruction? lsl $r7, $r7,1	
2. The function field is used to identify the operations that happen in the ALU for branch instructions (T/F)	
3. Where does the LW instruction write the result?	
4. How many memories are present in the MIPS single-cycle data-path?	
5. Identify the register where there exists a RAW hazard: add $1, $2, $3; add $3, $1, $2;	
6. The PCsrc control signal is used for writing in the Program Counter. (T/F)	
7. How many read accesses does a register file have?	
8. What type of control unit is used in MIPS single-cycle?	
9. In pipeline MIPS, where is the result of the BEQ instruction written (when the branch condition is true)?	
10. How many clock cycles are necessary to execute 150 instructions in MIPS pipeline?	
11. A processor that supports the execution of more instructions in one clock cycle is …	
12. The micro-programmed control unit uses a PLA to generate the control signals. (T/F)	
13. The 3 address machine is called accumulator. (T/F)	
14. A Harvard architecture has separate memories for Instructions and Data. (T/F)	
15. The jump instruction uses PC absolute addressing. (T/F)	
16. What is the pipeline register where the RegWrite control signal is coming from?	
17. In speculative Tomasulo, the store buffers hold the address and data to be written to memory (T/F).	
18. For a cache hit, one must compare the …	
19. A branch target buffer (BTB) is a cache memory that stores virtual addresses. (T/F)	
20. Write policy: Writing in the cache and also in the main memory is called …	

(T/F) = True or False

II. Using HLS, design a circuit that implements the following equation: $x = a + \frac{b}{4} + 8 \bullet c$ with the following constraints: **1 ALU**. Draw the data-path of the circuit using a mux based architecture. Write the RTL concrete, highlighting the values of the control signals. **(1.5 p)**

III. Modify the Multi-cycle MIPS CPU for the following instructions: **BLTZ** (branch on less than zero), **SLL** (shift left logical), **JAL** (jump and link). Define the instruction formats, write the **RTL Abstract and Concrete** for **all** the required instructions. Draw the **modified** data-path. Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. Draw the pipeline diagram **with and without forwarding** for the following code sequence: **lw $10, 10($6); sw $6, 5($3); xor $6, $10, $6; add $3, $10, $6; sw $3, 10($6).** Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence **in the two configurations**. **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 1 MB cache memory for this CPU. The block size is 128 bytes. Show the block diagram, and the address decoding for **a direct mapped cache** memory and **a 4-way set associative cache** memory. **(1.0 p)**

CA Exam, 16.06.2023 – English, R2 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. Suppose the value 0x35 is loaded in RF[7]. What is the value in RF[7] after the execution of the following instruction? lsr $r7, $r7,1	
2. What is the minimum amount of data that can be accessed in a memory?	
3. The shift amount is used in the sllv instructions. (T/F)	
4. How many memories are present in the MIPS multi-cycle data-path?	
5. Identify the register where there exists a RAW hazard: add $5, $2, $3; sw $3, 6($5)	
6. The reads of the register file in MIPS single-cycle are synchronous. (T/F)	
7. A Von Neumann architecture has separate memories for Instructions and Data. (T/F)	
8. What type of control unit is used in MIPS multi-cycle?	
9. How many clock cycles one must stall for resolving the Load Data Hazard in MIPS pipeline?	
10. How many clock cycles are necessary to execute 56 instructions in MIPS pipeline?	
11. For forwarding, one must set to 0 the write control signals for the register file and data memory in MIPS pipeline. (T/F)	
12. The execution of instructions before it is known if it is safe to do so is called …	
13. For which instruction is the MemWrite control signal asserted?	
14. What operation is performed in Booth's algorithm when a beginning of run of 1s occurs?	
15. In the global branch prediction scheme, a branch target buffer is used for indexing in the history table. (T/F)	
16. Where does the store information (store address + store data) come from in the Speculative Tomasulo method?	
17. CDB conflicts can appear in the Scoreboard method. (T/F)	
18. If a location is not valid in the cache, a cache …. occurs.	
19. How is the data organized in the main memory?	
20. A page fault is a miss in virtual memory. (T/F)	

(T/F) = True or False

II. Using HLS, design a circuit that implements the following equation: $x = a^2 - 2 \bullet a \bullet b + b^2$ with the following constraints: 1 ALU and 1 multiplier. Draw the data-path of the circuit using a mux based architecture. Write the RTL concrete, highlighting the values of the control signals. **(1.5 p)**

III. Modify the Multi-cycle MIPS CPU for the following instructions: **BGTZ** (branch on greater than zero), **SLTI** (Set on less than immediate), **JR** (jump register). Define the instruction formats, write the **RTL Abstract and Concrete** for **all** the required instructions. Draw the **modified** data-path. Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. Draw the pipeline diagram **with and without forwarding** for the following code sequence: **sw $5, 100($2); lw $2, 10($5); add $2, $5, $2; or $5, $5, $2; sw $5, 10($2); lw $7, 20($5).** Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence **in the two configurations**. **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 512 KB cache memory for this CPU. The block size is 32 bytes. Show the block diagram, and the address decoding for **a direct mapped cache** memory and **a 2-way set associative cache** memory. **(1.0 p)**