CA Exam, 06.07.2023 – English, R1 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. What is the minimum amount of data that can be accessed in a memory?	
2. The function field is used to identify the operations that happen in the ALU for R-type instructions (T/F)	
3. Where does the SW instruction write the result?	
4. The shift amount is used in the sll instructions. (T/F)	
5. Identify the register where there exists a RAW hazard: sub $4, $2, $6; add $6, $4, $2;	
6. The PCsrc control signal is used for writing in the Program Counter. (T/F)	
7. The jump instruction uses PC relative addressing. (T/F)	
8. The micro-programmed control unit uses a memory for storing the values of the control signals. (T/F)	
9. In pipeline MIPS, where is the result of the BEQ instruction written (when the branch condition is true)?	
10. How many clock cycles are necessary to execute 110 instructions in MIPS pipeline, if there are no data dependencies?	
11. Give an example of a 2 address machine architecture.	
12. If a location is not valid in the cache, a cache …. occurs.	
13. What is the pipeline register where ALUSrc control signal is coming from?	
14. In classical Tomasulo, the store buffers hold the address and data to be written to memory (T/F).	
15. The reorder buffer holds the instructions in the order they were issued in Speculative Tomasulo. (T/F)	
16. The BHT is a table of 2-bit counters indexed by a subset of the PC. (T/F)	
17. The GShare branch predictor uses a local history table. (T/F)	
18. An architecture that dispatches more instructions in one clock cycle is called …	
19. In which set can block 14 be written in a 4 way set associative cache?	
20. “Move blocks consisting of contiguous words to the upper levels” is called … locality.	

(T/F) = True or False

II. Describe the Booth multiplication algorithm. Present the Booth principle, ASM diagram, data-path and give a numerical example. **(1.5 p)**

III. Modify the Multi-cycle MIPS CPU for the following instructions: **BGTZAL** (branch on greater than zero and link), **SRLV** (shift right logical by variable), **XORI** (XOR immediate). Define the instruction formats, write the **RTL Abstract and Concrete** for **all** the required instructions. Draw the **modified** data-path. Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. Draw the pipeline diagram **with and without forwarding** for the following code sequence: **sw $7, 100($2); lw $2, 50($7); sw $2, 100($7); add $2, $2, $7; lw $7, 100($2); xor $2, $7, $2.** Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence **in the two configurations**. **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a 256 KB cache memory for this CPU. The block size is 64 bytes. Show the block diagram, and the address decoding for **a direct mapped cache** memory and **a 4-way set associative cache** memory. **(1.0 p)**