CA Exam, 21.06.2024 – English, R1 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. The 1 address machine is called Stack (T/F).	
2. A pipeline system is optimized for latency (T/F).	
3. A multi-cycle system is optimized for instruction throughput (T/F).	
4. What is the maximum number of instructions that can be encoded in MIPS?	
5. The control unit in the single-cycle MIPS is implemented with a PLA (T/F).	
6. For R-type instructions the function field determines the ALU operation (T/F).	
7. What is the logic gate for computing overflow in the MSB in the ALU?	
8. WAR data hazards can appear in the pipeline MIPS (T/F).	
9. The branch instruction uses PC relative addressing (T/F).	
10. How many clock cycles are necessary to execute **187** instructions in pipeline MIPS, if there are no data dependencies?	
11. The RegDst control signal is used for writing in the Register File (T/F).	
12. In pipeline MIPS, using the result before it was written is called …	
13. In multi-cycle MIPS the JMP instruction takes 3 clock cycles (T/F).	
14. In static branch prediction the branch history decides the direction of the branch (T/F).	
15. The amount of data transferred between the cache memory and the physical memory and is called a …	
16. In which block can one place the data block no. **63** (from main memory) in **a direct mapped cache** memory with **32 blocks**?	
17. The data structure used to implement the reorder buffer (ROB) in Speculative Tomasulo is a FIFO (T/F).	
18. The instructions in Tomasulo always complete in order (T/F).	
19. A branch target buffer (BTB) stores the branch target address (T/F).	
20. The Page Table is a cache memory that stores virtual addresses. (T/F)	

(T/F) = True or False

II. Design a **32-bit ALU** for the following operations: **ADD, SUB, NAND, NOR, Negate A, Increment A, Decrement A, SLT**. Design the **1-bit ALU** by using a single adder circuit and then extend it in order to obtain the 32-bit ALU. Draw the schematic with control signals and present a table with the control signal values for the required operations. **(1.5 p)**

III. Modify the **single-cycle** MIPS CPU for the following instructions: **SWAP** (exchange the contents of two registers), **BLEZ** (branch on less than or equal to zero), **JALR** (jump and link register). Define the instruction formats, write the **RTL Abstract** for **all** the required instructions. Draw the **modified** data-path (all the normal instructions should work). Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. Draw the pipeline diagram **with and without forwarding** for the following code sequence: **LW R2, 100 (R3); SW R2, 400(R3); ORI R4, R2, #100; ADD R9, R2, R4; SUB R3, R9, R2; BNE R3, R9, #4;** Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence **in the two configurations**. **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a **128 KB** cache memory for this CPU. The block size is **64 bytes**. Show the block diagram, and the address decoding for **a direct mapped cache** memory and **a 2-way set associative cache** memory. **(1.0 p)**

CA Exam, 21.06.2024 – English, R2 **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. MIPS is a 2 address machine (T/F).	
2. How many registers does a MIPS register file have?	
3. The Microprogrammed control unit uses a memory to generate the control signals (T/F).	
4. What is the maximum number of R–type instructions that can be encoded in MIPS?	
5. The result of **SLT** is 1 if the first operand is greater than the second operand (T/F).	
6. The PCSrc control signal is used for writing in the Program Counter (T/F).	
7. In multi-cycle MIPS the ALUOut register stores the branch address before the branch outcome is known (T/F).	
8. In multi-cycle MIPS, where is the result of the BEQ instruction written (when the branch condition is true)?	
9. In the pipeline MIPS, the branch address is computed in the ALU (T/F).	
10. The one flip-flop per state control unit can be derived from the FSM based one (T/F).	
11. Forcing to **0** the control signals in the pipeline is called stalling (T/F).	
12. What is the pipeline register where the RegWrite control signal is coming from?	
13. CDB conflict can appear in Scoreboarding (T/F).	
14. An architecture that dispatches more instructions / clock cycle is called ...	
15. In which set can one place the data block no. **63** (from main memory) in a **4-way set-associative cache** memory with **32 blocks**?	
16. The dirty-bit = 1 indicates a write in the cache memory block. (T/F)	
17. The amount of data transferred between the physical memory and the hard disk is called a …	
18. The instructions in Speculative Tomasulo always complete in order (T/F).	
19. The bimodal branch prediction uses a branch history table indexed by the branch target address (T/F).	
20. The Page Table Implements Virtual to Physical Address Translation (T/F).	

(T/F) = True or False

II. Design a **32-bit ALU** for the following operations: **ADD, SUB, Increment A and Decrement A;** for 1 operation on 32-bit operands, 2 operations on 16-bit operands or 4 operations on 8-bit operands (MMX). Draw the schematic with control signals using **four 8-bit adders** and the necessary auxiliary circuits. Show a table with the values of the control signals for the required operations. **(1.5 p)**

III. Modify the **single-cycle** MIPS CPU for the following instructions: **SWAPM** (exchange the contents of a register with a memory location), **BGEZAL** (Branch on greater than or equal to zero and link), **SUBI** (subtract immediate). Define the instruction formats, write the **RTL Abstract** for **all** the required instructions. Draw the **modified** data-path (all the normal instructions should work). Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. Draw the pipeline diagram **with and without forwarding** for the following code sequence: **LW R1, 0(R2); ADDI R1, R1, #1; SW R1, 0(R2); ADDI R2, R2, #4; SUB R4, R3, R2; BNE R4, R5, #8;** Identify and explain the hazards in the code sequence and how they are resolved. Specify how many clock cycles does it take to execute the code sequence **in the two configurations**. **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a **256 KB** cache memory for this CPU. The block size is **128 bytes**. Show the block diagram, and the address decoding for **a direct mapped cache** memory and **a 2-way set associative cache** memory. **(1.0 p)**