CA Exam, 10.07.2024 – English **Student Name:** _____

Year: _____ **Group:** _____

I. Answer the following questions using only one word, or one number. Write the answers in the table: **(4.0 p)**

1. MIPS is a 3 address machine (T/F).	
2. A pipeline system is optimized for latency (T/F).	
3. The Microprogrammed control unit uses a PLA to generate the control signals (T/F).	
4. What is the maximum number of R–type instructions that can be encoded in MIPS?	
5. The result of **SLT** is 1 if the first operand is equal to the second operand (T/F).	
6. The PCSrc control signal is used for writing in the Program Counter (T/F).	
7. What is the logic gate for computing overflow in the MSB in the ALU?	
8. In multi-cycle MIPS, where is the result of the BEQ instruction written (when the branch condition is true)?	
9. The branch instruction uses PC relative addressing (T/F).	
10. How many clock cycles are necessary to execute **256** instructions in pipeline MIPS, if there are no data dependencies?	
11. Forcing to **0** the control signals in the pipeline is called stalling (T/F).	
12. What is the pipeline register where the RegWrite control signal is coming from?	
13. In pipeline MIPS, using the result before it was written is called …	
14. An architecture that dispatches more instructions / clock cycle is called ...	
15. In which set can one place the data block no. **50** (from main memory) in a **4-way set-associative cache** memory with **32 blocks**?	
16. The data structure used to implement the reorder buffer (ROB) in Speculative Tomasulo is a Heap (T/F).	
17. The amount of data transferred between the physical memory and the hard disk is called a …	
18. The instructions in Speculative Tomasulo always commit in order (T/F).	
19. The bimodal branch prediction uses a branch history table indexed by the lower bits of the branch target address (T/F).	
20. In static branch prediction the branch history decides the direction of the branch (T/F).	

(T/F) = True or False

II. Design a **32-bit ALU** for the following operations: **ADD, SUB, AND, OR, NAND, NOR, Negate B, Increment B, Decrement B**. Explain how each ALU operation is implemented. Design the **1-bit ALU** by using a single adder circuit and then extend it in order to obtain the **32-bit ALU**. Draw the schematic with control signals and present a table with the control signal values for the required operations. **(1.5 p)**

III. Modify the **multi-cycle** MIPS CPU for the following instructions: **SWAP** (exchange the contents of two registers), **SWAPM** (exchange the contents of a register with a memory location), **BLTZAL** (Branch on less than and link). Define the instruction formats, write the **RTL Abstract and Concrete** for **all** the required instructions. Draw the **modified** data-path (all the normal instructions should work). Show the control signals and their values for implementing the required instructions. **(2.5 p)**

IV. A MIPS CPU has the following resources: 1 Integer Unit, 2 FP Add Units, 1 FP MUL Unit, 1 FP DIV Unit; Execution times (clock cycles): Integer Unit – 1, FP Add – 4, FP MUL – 10, FP DIV – 40. Identify the hazards and trace the following instructions using the classic Tomasulo Algorithm (draw and fill the table): **LD F6, 12(R2); SD F6, 16(R3); MULD F8, F6, F2; ADDD F1, F5, F4; DIVD F8, F1, F6; ADDD F6, F8, F2; ADDD F1, F3, F2** **(1.0 p)**

V. A 32-bit CPU generates 32-bit addresses for a byte addressable memory. Design a **64 KB** cache memory for this CPU. The block size is **128 bytes**. Show the block diagram, and the address decoding for **a direct mapped cache** memory and **a 2-way set associative cache** memory. **(1.0 p)**